GOVERNMENT COLLEGE OF ENGINEERING

(An Autonomous Institution Affiliated to Anna University)

BARGUR-635104

Curriculum and Syllabus
For

M.E- APPLIED ELECTRONICS
(Full Time)

I TO IV SEMESTERS

2018

Regulation

OFFICE OF CONTROLLER OF EXAMINATIONS

GOVERNMENT COLLEGE OF ENGINEERING

BARGUR – 635 104

Website: www.gcebargur.ac.in

PROGRAMME SPECIFIC OUTCOMES	
1.	To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, communications, digital system design, embedded systems and VLSI design.
2.	To develop electronic systems using modern engineering hardware and software tools.
3.	To work professionally and ethically in applied electronics and allied areas.
PROGRAM EDUCATIONAL OBJECTIVES	
1.	Ability to acquire in-depth knowledge in the field of Electronics with a ability to evaluate and analyse the existing knowledge for enhancement.
2.	Ability to analyse critical complex engineering problems and provide solutions through research.
3.	Ability to think latterly and solve engineering problems optimally considering public health and safety, cultural and societal factors in the core areas.
4.	Ability to extract information pertinent to challenging problems through literature survey and by appropriate research methodologies, techniques and tools to the development of technological knowledge.
5.	Ability to select, learn and apply appropriate techniques, resources and modern engineering tools to complex engineering activities with an understanding of limitations
6.	Ability to understand group dynamics, recognize opportunities and contribute positively to multidisciplinary work to achieve common goals for further learning.
7.	Ability to demonstrate engineering principles and apply the same to manage projects efficiently as a team after considering economical and financial factors.
8.	Ability to communicate with engineering community and society regarding complex engineering activities effectively through reports, design documentation and presentation.
9.	Ability to encage with commitment in life-long learning independently to improve knowledge and competence.
10.	Ability to acquire professional and intellectual integrity, professional code and contact, ethics of research and scholarship by considering the research outcomes to the community for sustainable development of society.
11.	Ability to observe and examine critically the outcomes and make corrective measures, and learn from mistakes without depending on external feedback.

M.E APPLIED ELECTRONICS (PG) CURRICULUM DESIGN

CREDIT SUMMARY

SL. NO	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS ACTUAL	% OF CREDITS	TOTAL NO. OF COURSES
		I	II	III	IV			
1.	**BS (FC)**	4				4	5.56	1
2.	**PC C**	15	14	5		34	47.22	12
3.	**PE C**	3	6	3		12	16.67	4
4.	**OEC**			3		3	4.16	1
5.	**EEC**		1	6	12	19	26.39	3
6.	**AC**	0	0	0		**0**	0	3
7.	**TOTAL**	**22**	**21**	**17**	**12**	**72**	**100**	**24**

GOVERNMENT COLLEGE OF ENGINEERING
BARGUR

Regulation – 2018

Full Time M.E.–Applied Electronics
(Department of ECE)

SEMESTER-I

SL. No.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C
THEORY								
1.	18AEFC01	Mathematical Foundations for Electronics Engineers	FC	4	4	0	0	4
2.	18AEPC02	Advanced Digital System Design	PCC	3	3	0	0	3
3.	18AEPC03	Advanced Digital Signal Processing	PCC	4	4	0	0	4
4.	18AEPC04	Embedded System Design	PCC	3	3	0	0	3
5.	18AEPC05	Modern communication techniques	PCC	3	3	0	0	3
6.		Professional Elective I	PCC	3	3	0	0	3
7.		Audit Course I	AC	2	2	0	0	0
PRACTICAL								
8.	18AEPC06	Electronic System Design Laboratory I	PCC	4	0	0	4	2
			TOTAL	**26**	**18**	**0**	**8**	**22**

SEMESTER-II

SL. No.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C
THEORY								
1.	18AEPC07	Soft Computing and Optimization Techniques	PCC	3	3	0	0	3
2.	18AEPC08	VLSI System Design	PCC	3	3	0	0	3
3.	18AEPC09	Digital Image Processing	PCC	3	3	0	0	3
4.	18AEPC10	Internet of Things	PCC	3	3	0	0	3
5.		Professional Elective II	PEC	3	3	0	0	3
6.		Professional Elective III	PEC	3	3	0	0	3
7.		Audit Course II	AC	2	2	0	0	0
PRACTICAL								
8.	18AEPC11	Electronic System Design Laboratory II	PCC	4	0	0	4	2
9.	18AEEE12	Term Paper Writing and Seminar	EEC	2	0	0	2	1
			TOTAL	**26**	**18**	**0**	**8**	**21**

SEMESTER-III

SL. No.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C
THEORY								
1.	18AEPC13	Electronic Product design and development	PCC	3	3	0	0	3
2.		Professional Elective IV	PEC	3	3	0	0	3
3.		Open Elective	OEC	3	3	0	0	3
4.	18ZAC003	Research Methodology and IPR	AC	2	2	0	0	0
PRACTICAL								
5.	18AEPC14	Electronic Product Design Laboratory	PCC	4	0	0	4	2
6.	18AEEE15	Project Work Phase I	EEC	12	0	0	12	6
			TOTAL	**27**	**11**	**0**	**16**	**17**

SEMESTER-IV

SL. No.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C
PRACTICAL								
1.	18AEEE16	Project Work Phase II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 72

LIST OF PROFESSIONAL ELECTIVES (PEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1.	18AEPE01	Digital Control Engineering	PEC	**2**	**1**	**0**	**3**
2.	18AEPE02	Computer Architecture	PEC	**3**	**0**	**0**	**3**
3.	18AEPE03	Digital VLSI design	PEC	**3**	**0**	**0**	**3**
4.	18AEPE04	Electromagnetic Interference and Compatibility	PEC	**3**	**0**	**0**	**3**
5.	18AEPE05	CAD for VLSI	PEC	**3**	**0**	**0**	**3**
6.	18AEPE06	Nano Electronics	PEC	**3**	**0**	**0**	**3**
7.	18AEPE07	Sensors and Signal Conditioning	PEC	**3**	**0**	**0**	**3**
8.	18AEPE08	MEMS and NEMS	PEC	**3**	**0**	**0**	**3**
9.	18AEPE09	DSP Processors Architecture and Programming	PEC	**3**	**0**	**0**	**3**
10.	18AEPE10	RF System Design	PEC	**2**	**1**	**0**	**3**
11.	18AEPE11	Speech Signal Processing	PEC	**2**	**1**	**0**	**3**
12.	18AEPE12	Solid State Device Modeling and simulation	PEC	**3**	**0**	**0**	**3**
13.	18AEPE13	Advanced Microprocessor and Microcontroller Architecture	PEC	**3**	**0**	**0**	**3**
14.	18AEPE14	System on Chip	PEC	**3**	**0**	**0**	**3**
15.	18AEPE15	Robotics	PEC	**3**	**0**	**0**	**3**
16.	18AEPE16	Physical Design of VLSI Circuits	PEC	**3**	**0**	**0**	**3**
17.	18AEPE17	High Performance Networks	PEC	**3**	**0**	**0**	**3**

18.	18AEPE18	Pattern Recognition	PEC	**3**	**0**	**0**	**3**
19.	18AEPE19	Secure Computing Systems	PEC	**3**	**0**	**0**	**3**
20.	18AEPE20	Signal Integrity for High Speed Design	PEC	**3**	**0**	**0**	**3**
21.	18AEPE21	Wireless AD-HOC and Sensor Networks	PEC	**3**	**0**	**0**	**3**
22.	18AEPE22	Hardware – Software Co-design	PEC	**3**	**0**	**0**	**3**

LIST OF OPEN ELECTIVES (OE)

SL. NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1	18AEOE01	Introduction to Nanoelectronics	OE	**3**	**0**	**0**	**3**
2	18AEOE02	Genetic Algorithms	OE	**3**	**0**	**0**	**3**
3	18AEOE03	Neural Networks	OE	**3**	**0**	**0**	**3**
4	18AEOE04	Multimedia Compression Techniques	OE	**3**	**0**	**0**	**3**

LIST OF AUDIT COURSES (AC)

SL. NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1	18ZAC001	Disaster Management	AC	**2**	**0**	**0**	**0**
2	18ZAC002	English for Research Paper Writing	AC	**2**	**0**	**0**	**0**
3	18ZAC003	Research Methodology and IPR	AC	**2**	**0**	**0**	**0**
4	18ZAC004	Sanskrit for Technical Knowledge	AC	**2**	**0**	**0**	**0**

5	18ZAC005	Value Education	AC	**2**	**0**	**0**	**0**
6	18ZAC006	Pedagogy Studies	AC	**2**	**0**	**0**	**0**
7	18ZAC007	Stress Management by Yoga	AC	**2**	**0**	**0**	**0**
8	18ZAC008	Personality Development through Life Enlightenment Skills	AC	**2**	**0**	**0**	**0**
9	18ZAC009	Electronic Waste Management	AC	**2**	**0**	**0**	**0**

LIST OF PROFESSIONAL CORE COURSES (PCC)

SL. NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	18AEPC02	Advanced Digital System Design	PCC	3	0	0	3
2.	18AEPC03	Advanced Digital Signal Processing	PCC	4	0	0	4
3.	18AEPC04	Embedded System Design	PCC	3	0	0	3
4.	18AEPC05	Modern Communication Techniques	PCC	3	0	0	3
5.	18AEPC06	Electronic System Design Laboratory I	PCC	0	0	4	2
6.	18AEPC07	Soft Computing and Optimization Techniques	PCC	3	0	0	3
7.	18AEPC08	VLSI System Design	PCC	3	0	0	3
8.	18AEPC09	Digital Image Processing	PCC	3	0	0	3
9.	18AEPC10	Internet of Things	PCC	3	0	0	3
10.	18AEPC11	Electronic System Design Laboratory II	PCC	0	0	4	2

11.	18AEPC13	Electronic Product design and development	PCC	3	0	0	3
12.	18AEPC14	Electronic Product design Lab	PCC	0	0	4	2

LIST OF EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SL.NO	COURSE CODE	COURSETITLE	CAT	L	T	P	C
1.	18AEEE12	Term Paper Writing and Seminar	EEC	0	0	2	1
2.	18AEEE15	Project Work Phase I	EEC	0	0	12	6
3.	18AEEE16	Project Work Phase II	EEC	0	0	24	12

LIST OF FOUNDATIONAL COURSES (FC)

SL.NO	COURSE CODE	COURSETITLE	CAT	L	T	P	C
1.	18AEFC01	Mathematical Foundations for Electronics Engineers	FC	4	0	0	4

EVALUATIONS :: 2018 REGULATIONS

Each course shall be evaluated for a maximum of 100 marks as shown below:

Sl. No	Category of course	Continuous Assessment	End-Semester Examinations
1.	Theory Courses	50 Marks	50 Marks
2.	Laboratory Courses	50 Marks	50 Marks
3.	Project Work	50 Marks	50 Marks
4.	All other EEC Courses (non theory)	100 Marks	-

Continuous Assessment Mark the following guidelines are to be followed.

Sl.No.	Category Details	CA Marks	Weightage
1.	Test (3 Nos.) {each test is to be conducted for 50 Marks}	30 Marks	60%
2.	Assignment (3 Nos.)	20 Marks	40%
	TOTAL	50 Marks	100%

Marks for Project Work and the Viva-Voce Examination / Term Paper Writing and Seminar will be distributed as indicated below.

Continuous Assessment 50 Marks				End Semester Examination 50 Marks		
Review I (25 Marks)		Review II (25 Marks)		Report Evaluation (20 Marks)	Viva-Voce (30 Marks)	
Review Committee (Excluding Guide)	Guide	Review Committee (Excluding Guide)	Guide	External Examiner	External Examiner	Internal Examiner **
15	10	15	10	20	15	15

**Guide will be the internal

A student has to **secure minimum of 75% attendance** for appearing end semester examination. If a student secures **65% to 75% attendance** in the Current Semester due to medical reasons (hospitalization / accident / specific illness) or due to participation in the College / University / State / National / International Level Sports events with prior permission from the Head of the Department concerned, the student shall apply for **condonation**. Condonation can be allowed only two semesters (i.e **only two condonations**) during the entire course of study**.**

Students who secure **less than 65% attendance** will **not be permitted to write the End-Semester Examination.**

SEMESTER I

18AEFC01	MATHEMATICAL FOUNDATIONS FOR ELECTRONICS ENGINEERS	L	T	P	C
		4	0	0	4

OBJECTIVES:

- To impart knowledge on fuzzy logic.
- To understand the basic concepts of matrix theory and their applications.
- To find the optimum solution of the random variables.
- To understand the concepts of dynamic programming and queuing models.

UNIT I	FUZZY LOGIC	12

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II	MATRIX THEORY	12

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization – Least squares method - Singular value decomposition.

UNIT III	PROBABILITY AND RANDOM VARIABLE	12

Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables -Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.

UNIT IV	DYNAMIC PROGRAMMING	12

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V	QUEUEING MODELS	12

Poisson Process – Markovian queues – Single and multi server models – Little's formula – Machine interference model – Steady state analysis – Self service queue.

TOTAL:60 PERIODS

OUTCOMES:

1.	Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy

	prepositions and fuzzy quantifiers and applications of fuzzy logic.
2.	Apply various methods in matrix theory to solve system of linear equations.
3.	Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
4.	Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
5.	Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models
6.	Using discrete time Markov chains to model computer systems.

REFERENCES:

1.	*Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.*
2.	*George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.*
3.	*Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.*
4.	*Johnson, R.A., Miller, I and Freund J., "Miller and Freund"s Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.*
5.	*Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia, NewDelhi, 2016.*

18AEPC02	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Introduce methods to analyze and design synchronous and asynchronous sequential circuit
- Introduce the architecture of programmable device
- Introduce design and implementation of digital circuits using programming tools

UNIT I	SEQUENTIAL CIRCUIT DESIGN	9

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM

UNIT II	ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of synchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS	9

Fault table method-path sensitization method – Boolean difference method-D algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT IV	SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES	9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL –Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 400

UNIT V	SYSTEM DESIGN USING VERILOG	9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench -Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Analyze sequential digital circuits
2.	design sequential digital circuits
3.	Identify the requirements and specifications of the system required for a given application
4.	Identify the requirements and specifications of the system required for a given application
5.	use programming tools for implementing digital circuits of industrial standard

REFERENCES:	
1.	*Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004*
2.	*M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.*
3.	*M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.*
4.	*Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001*
5.	*Parag K.Lala "Digital system Design using PLD" B S Publications,2003*
6.	*Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002*
7.	*S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	-	-	-	-	-	-	3	-	3	2	-
CO2	2	3	2	-	-	-	-	-	-	2	-	3	2	-
CO3	3	2	2	-	-	2	-	-	-	1	1	3	2	-
CO4	3	3	2	-	-	2	-	-	-	2	-	3	2	-
CO5	2	2	2	-	-	-	-	-	-	2	-	3	2	-
	3	3	2	-	-	2	-	-	-	2	1	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC03	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		4	0	0	4

OBJECTIVES

1. To introduce the basics of random signal processing and spectral estimation

2. To understand the concepts of estimation and prediction of non stationary signals.

3. To learn about adaptive filtering and multirate signal processing.

UNIT I	DISCRETE RANDOM SIGNAL PROCESSING	12

Discrete Random Processes – Ensemble averages -Wide sense stationary process –Auto-correlation and Auto- covariance matrices - Properties – Parseval's Theorem -Weiner Khintchine relation - Power spectral density – Filtering random process, Spectral Factorization - White noise -Simulation of uniformly distributed/Gaussian distributed white noise – Simulation of Sine wave mixed with Additive White Gaussian Noise.

UNIT II	SPECTRUM ESTIMATION	12

Bias and Consistency of estimators - Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysis of estimators –Periodogram–Modified Periodogram, Barlettmethod - Welch estimation, Blackman Tukey method.Parametric methods: Model based approach - AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker equations, Solutions using Durbin's algorithm.

UNIT III	LINEAR ESTIMATION AND PREDICTION	12

Linear prediction – Forward prediction and Backward prediction– Levinson Durbin recursion algorithm - Wiener filter - FIR Wiener filter- Filtering and linear prediction, non-causal and causal IIR Wiener filters - DiscreteKalman filter.

UNIT IV	ADAPTIVE FILTERS	12

FIR Adaptive filters - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS – Sliding window RLS.

UNIT V	MULTIRATE DIGITAL SIGNAL PROCESSING	12

Mathematical description of change of sampling rate – Interpolation and Decimation-Decimation by an integer factor – Interpolation by an integer factor – Sampling rate conversion by a rational factor –Filter implementation for sampling rate conversion- direct form FIR

structures, Polyphase filter structures, time variant structures – Multistage implementation of multirate system.	
	TOTAL: 60HOURS
OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Uunderstand the basics of random signal processing
2.	Analyse the spectral estimation of finite duration signals
3.	Uunderstand the linear estimation and prediction of non stationary signals.
4.	Able to design adaptive filters and use them in relevant applications
5.	Acquire knowledge on multirate signal processing and implement the multirate filters.
REFERENCES:	
1.	*Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2006.*
2.	*John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India, New Delhi, 2005.*
3.	*P. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1992.*
4.	*S. Kay," Modern spectrum Estimation theory and application", Prentice Hall, Englehood Cliffs, NJ1988.*
5.	*Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986*
6.	*Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	-	1	1	-	2	-	1	-	-	2	-	1
CO2	2	2	-	2	1	-	2	-	1	-	-	2	-	1
CO3	2	2	-	2	1	-	1	-	1	-	-	2	-	1
CO4	2	2	-	2	2	-	1	-	1	-	-	2	2	1
CO5	2	2	-	2	2	-	1	-	1	-	-	2	2	1
	2	2	-	2	1	-	1	-	1	-	-	2	1	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC04	EMBEDDED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the design challenges about embedded system.
- To learn various techniques of system processor.
- To understand different state machine and process models.

UNIT I	EMBEDDED SYSTEM OVERVIEW	9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II	GENERAL AND SINGLE PURPOSE PROCESSOR	9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III	BUS STRUCTURES	9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV	STATE MACHINE AND CONCURRENT PROCESS MODELS	9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS..

	TOTAL : 45 PERIODS

OUTCOMES:	Upon the course completion, the student will have the ability
1.	To explain the embedded system design challenges and its optimization
2.	To explain single purpose processor and its internal peripherals.
3.	To compare bus architecture for interfacing and communication protocols.
4.	To discuss state machine and design process models
5.	To outline embedded software development tools and RTOS

REFERENCES:	
1.	*Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.*
2.	*Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.*
3.	*Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.*
4.	*Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	-	1	1	-	2	-	1	-	-	2	-	1
CO2	2	2	-	2	1	-	2	-	1	-	-	2	-	1
CO3	2	2	-	2	1	-	1	-	1	-	-	2	-	1
CO4	2	2	-	2	2	-	1	-	1	-	-	2	2	1
CO5	2	2	-	2	2	-	1	-	1	-	-	2	2	1
	2	2	-	2	1	-	1	-	1	-	-	2	1	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC05	MODERN COMMUNICATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the coherent and non-coherent receivers and its impact on different channel characteristics
- To understand the operation of different Equalizers
- To understand the different block coded and convolutional coded digital communication systems

UNIT I	POWER SPECTRUM AND COMMUNICATION OVER MEMORYLESS CHANNEL	9

PSD of a Synchronous Data Pulse Stream – M–ary Markov source – Convolutionaly Coded Modulation – Continuous Phase Modulation – Scalar and Vector Communication over Memory less Channel – Detection Criteria.

UNIT II	COHERENT AND NON –COHERENT COMMUNICATION	9

Coherent Receivers – Optimum Receivers in WGN – IQ Modulation & Demodulation – Non–Coherent receivers in Random Phase Channels – M–FSK Receivers – Rayleigh and Rician Channels – Partially Coherent Receivers – DPSK – M –PSK – M –DPSK – BER Performance Analysis.

UNIT III	BANDLIMITED CHANNELS AND DIGITAL MODULATIONS	9

Eye pattern – Demodulation in the presence of ISI and AWGN – Equalization techniques – IQ modulations – QPSK – QAM – QBOM – BER Performance Analysis – Continuous Phase Modulation – CPFM – CPFSK – MSK – OFDM

UNIT IV	BLOCK CODED DIGITAL COMMUNICATION	9

Architecture and Performance – Binary Block Codes – Orthogonal – Bi–orthogonal – Trans–orthogonal – Shannon's Channel Coding Theorem – Channel Capacity – Matched Filter – Concepts of Spread Spectrum Communication – Coded BPSK and DPSK Demodulators – Linear Block Codes – Hamming–Golay Cyclic – BCH – Reed– Solomon Codes

UNIT V	CONVOLUTIONAL CODED DIGITAL COMMUNICATION	9

Representation of Codes using Polynomial – State Diagram – Tree Diagram and Trellis Diagram

– Decoding Techniques using Maximum Likelihood – Viterbi Algorithm – Sequential and Threshold methods – Error probability performance for BPSK and Viterbi Algorithm – Turbo Coding	
	TOTAL : 45 PERIODS
OUTCOMES:	Upon the course completion, the student will have the ability
1.	to analyze PSD of different sources.
2.	to compare coherent and non-coherent receivers for different channels.
3.	to compare different digital modulations over band limited channels.
4.	to analyze the performance of different block codes.
5.	to explain decoding techniques for convolutional coded digital modulation.
REFERENCES:	
1.	*Simon M. K., Hinedi S. M. and Lindsey W. C., "Digital Communication Techniques, Signaling and Detection", Prentice Hall India, 1995.*
2.	*Simon Haykin, "Digital communications", John Wiley and Sons, 1998.*
3.	*John G. Proakis, "Digital Communication", Fifth Edition, Mc Graw Hill Publication, 2008.*
4.	*Bernard Sklar, "Digital Communications", second edition, Pearson Education, 2001.*
5.	*Wayne Tomasi, "Advanced Electronic Communication Systems", 4th Edition Pearson Education , 1998.*
6.	*Lathi B. P., "Modern Digital and Analog Communication Systems", 3rd Edition, Oxford University Press, 1998.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	2	2	1	-	-	2	-	1	2	1	1
CO2	3	2	-	2	2	1	-	-	2	-	1	2	1	1
CO3	3	2	-	2	2	1	-	-	2	-	1	2	1	1
CO4	3	2	-	2	2	1	-	-	2	-	1	2	1	1
CO5	3	2	-	2	2	1	-	-	2	-	1	2	1	1
	3	2	-	2	2	1	-	-	2	-	1	2	1	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC06	ELECTRONIC SYSTEM DESIGN LABORATORY I	L	T	P	C
		0	0	4	2

Objectives:

- To learn about the embedded hardware
- To become familiar with various interfacing techniques
- To learn about the implementation of functional modules in FPGA

LIST OF EXPERIMENTS USING ARM PROCESSOR:

1.	Interfacing EEPROM using I^2C.
2.	Interfacing RF Transceiver using UART.
3.	Interfacing DC motor & speed control using PWM.
4.	Interfacing Temperature sensor using I^2C.
5.	Interfacing of Graphical LCD module.
6.	Interfacing of RTC.
7.	Interfacing of Stepper Motor.
8.	Programming in RTOS environment
9.	Data acquisition from a remote location and display using graphical LCD.
10.	Implementation of Linear convolution using FPGA.
11.	Implementation of FFT using FPGA.
12.	Design of closed loop system using PROTEUS software.
	TOTAL : 60 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Apply various interfacing techniques using ARM processor.
2.	Demonstrate various communication protocols.
3.	Design a system and validate using RTOS

4.	Design and analyze of real time system.
5.	Design and implementation of mathematical modules in FPGAs

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**3**	**-**	**-**	**1**	**2**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**-**	**-**
CO2	**2**	**2**	**-**	**-**	**3**	**-**	**1**	**1**	**-**	**-**	**-**	**-**	**2**	**-**
CO3	**2**	**3**	**-**	**-**	**3**	**-**	**-**	**2**	**-**	**-**	**1**	**3**	**2**	**-**
CO4	**2**	**3**	**-**	**1**	**3**	**-**	**3**	**2**	**-**	**-**	**3**	**3**	**1**	**-**
CO5	**2**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**3**	**3**	**2**
18AEPC06	**2**	**2**	**-**	**-**	**3**	**-**	**2**	**2**	**-**	**-**	**-**	**3**	**2**	**-**

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

SEMESTER II

18AEPC07	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

•	Learn the basics concepts of Soft Computing
•	become familiar with various techniques like neural networks , genetic algorithms and fuzzy systems.
•	Apply soft computing techniques to solve problems

UNIT I	NEURAL NETWORKS	9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network

UNIT II	FUZZY LOGIC	9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions- Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

UNIT III	NEURO-FUZZY MODELING	9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

UNIT IV	CONVENTIONAL OPTIMIZATION TECHNIQUES	9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization – sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V	EVOLUTIONARY OPTIMIZATION TECHNIQUES	9

Genetic algorithm - working principle, Basic operators and Terminologies, Building block

hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.	
	TOTAL : 45 PERIODS
OUTCOMES:	Upon completion the course , the students will have the ability to
1.	apply suitable soft computing techniques for various application
2.	Integrate various soft computing techniques for complex problems.
3.	Implement machine learning through neural networks
4.	develop a fuzzy expert system , model neuro fuzzy system for clustering and classification
5.	able to use the optimization techniques to solve the real world problem
REFERENCES:	
1.	*David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.*
2.	*George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.*
3.	*James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.*
4.	*Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.*
5.	*Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.*
6.	*Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.*
7.	*Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley & sons, inc,Fourth Edition, 2009*
8.	*Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.*
9.	*Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced Optimization Techniques, Springer 2012.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3	2	-	-	-	-	-	-	2	-	-	2	2	-
CO2	3	3	3	-	-	-	-	-	-	3	-	-	3	3	-
CO3	2	2	-	-	-	-	-	-	-	1	-	-	3	2	-
CO4	2	3	2	-	2	2	-	-	-	2	2	-	3	2	-
CO5	3	2	2	-	-	-	-	-	-	-	-	-	3	2	-
18LPC303	2	3	2	-	-	1	-	-	-	2	1	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC08	**VLSI SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To study different types of programming technologies and logic devices.
- To gain knowledge about partitioning, floor planning and routing including circuit extraction of ASIC
- To know about different high performance algorithms and its applications in ASICs.

UNIT I	**OVERVIEW OF ASIC AND PLD**	**9**

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II	**ASIC PHYSICAL DESIGN**	**9**

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC.

UNIT III	LOGIC SYNTHESIS, SIMULATION AND TESTING	9
Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.		
UNIT IV	**FIELD PROGRAMMABLE GATE ARRAYS**	**9**
FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.		
UNIT V	**SOC DESIGN**	**9**
System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Understand various programming technologies and logic devices
2.	Discuss about different floor planning and placement techniques.
3.	Analyze the synthesis, simulation and testing of systems.
4.	Apply different high performance algorithms in ASICs.
5.	Discuss the design issues of SOC.

REFERENCES:	
1.	*M.J.S.Smith, "Application - Specific Integrated Circuits", Pearson, 2003.*
2.	*Steve Kilts "Advanced FPGA Design" , Wiley Inter-Science, 2007.*
3.	*J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley& Sons, 1995.*
4.	*P.K.Chan & S. Mourad, "Digital Design using Field Programmable Gate Array", Prentice Hall, 1994.*
5.	*Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008.*
6.	*S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Pub., 1994.*

7.	*S.Brown,R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Pub.,1992.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	_	_	_	_	2	_	2	2	2	_
CO2	3	2	2	2	_	_	_	_	2	_	2	2	2	_
CO3	3	3	2	2	_	_	_	_	2	_	2	3	3	_
CO4	3	3	2	2	_	_	_	_	2	_	2	3	3	_
CO5	3	2	2	2	_	_	_	_	2	_	2	2	2	_
18AEPC08	3	2	2	2	_	_	_	_	2	_	2	2	2	_

1-Low 2—Moderate (Medium) 3-High

18AEPC09	**DIGITAL IMAGE PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Objectives:

- Understand fundamental of digital image
- Learn different image transforms
- Study concept of segmentation

UNIT I	**FUNDAMENTALS OF DIGITAL IMAGE PROCESSING**	**9**

Elements of visual perception-brightness, contrast, hue, saturation, mach band effect- 2D image transforms-DFT, DCT, KLT,SVD. Image enhancement in spatial and frequency domain-Review of Morphological image processing.

UNIT II	**SEGMENTATION**	**9**

Edge detection -Thresholding, Region growing- Fuzzy clustering-Watershed algorithm-Active contour models- Texture feature based segmentation-Graph based segmentation- Wavelet based Segmentation - Applications of image segmentation.

UNIT III	FEATURE EXTRACTION	9
First and second order edge detection operators-Phase congruency- Localized feature extraction - detecting image curvature, shape features, Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.		
UNIT IV	**REGISTRATION AND IMAGE FUSION**	**9**
Registration - Preprocessing, Feature selection - points, lines, regions and templates Feature correspondence - Point pattern matching, Line matching, Region matching, Template matching. Transformation functions - Similarity transformation and Affine Transformation. Resampling – Nearest Neighbour and Cubic Splines. Image Fusion - Overview of image fusion, pixel fusion, wavelet based fusion -region based fusion.		
UNIT V	**3D IMAGE VISUALIZATION**	**9**
Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiple connected surfaces, Image processing in 3D, Measurements on 3D images		
	TOTAL: 45 PERIODS	

COURSE OUTCOMES:	Upon completion the course , the students will have the ability
1.	To understand the image fundamentals.
2.	To understand the various image segmentation techniques.
3.	To extract features for image analysis.
4.	To introduce the concepts of image registration and image fusion.
5.	To illustrate 3D image visualization.

REFERENCES:

1.	*Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education,Inc., 2002.*
2.	*Ardeshir Goshtasby, " 2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications",John Wiley and Sons,2005.*
3.	*John C.Russ, "The Image Processing Handbook", CRC Press,2007.*
4.	*Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.*
5.	*Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson,Education, Inc.,Second Edition, 2004.*

6.	*Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis,2006.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	1	1	_	3	2	_	2	2	1	_
CO2	2	2	3	2	2	1	_	2	1	_	1	2	2	_
CO3	3	2	3	2	1	1	_	2	1	_	2	2	2	1
CO4	3	3	2	2	_	_	_	_	2	_	2	3	2	_
CO5	3	2	2	2	2	2	1	3	2	_	2	2	2	2
18AEPC09	3	3	2	2	1	2	_	3	2	_	2	2	2	2

1-Low 2—Moderate (Medium) 3-High

18AEPC10	**INTERNET OF THINGS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- Understand the fundamentals of Internet of Things and its protocols.
- Explore and learn about Internet of Things with help of preparing projects designed for Raspberry Pi.
- Realize the concept of Internet of Things in the real world scenario

UNIT I	**INTRODUCTION TO IoT**	**9**

Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

UNIT II	**IoT ARCHITECTURE**	**9**

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture

UNIT III	IoT PROTOCOLS	9
Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – LowPAN - CoAP – Security		
UNIT IV	**BUILDING IoT WITH RASPBERRY PI&ARDUINO**	**9**
Building IOT with RASPERRY Pi- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino.		
UNIT V	**SIMULATION OF DEVICES**	**9**
Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.		
	TOTAL : 45 PERIODS	

COURSE OUTCOMES:	Upon the course completion, the student will have the ability
1.	To analyze various protocols for IoT.
2.	To develop web services to access / control IoT devices.
3.	Ability to design a portable IoT using Raspberry Pi.
4.	To deploy an IoT application and connect to the cloud.
5.	Analyze applications of IoT in real time scenario.

REFERENCES:

1.	*HwaiyuGeng, "Internet of Things and Data Analytics", Wiley Publications, 2017.*
2.	*Srinivasa K G, "Internet of Things", CENCAGE Leaning India, 2017.*
3.	*Raj Kamal, "Internet of Things Architecture and Design Principles", Tata McGraw Hill, 2017.*
4.	*Arshdeep Bahga, Vijay Madisetti, "Internet of Things – A hands-on approach", Universities Press, 2015*
5.	*Olivier Hersent, David Boswarthick, Omar Elloumi , "The Internet of Things – Key applications and Protocols", Wiley, 2012*
6.	*Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.*

7.	*Jan Holler, Vlasios Tsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	-	-	3	-	2	2	1	2
CO2	2	2	2	2	2	3	-	-	3	-	2	2	2	2
CO3	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO4	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO5	2	2	2	3	3	3	-	-	3	-	2	3	3	2
	2	2	2	3	3	3	-	-	3	-	2	3	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC11	**ELECTRONIC SYSTEM DESIGN LABORATORY II**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

Objectives:

- To have a brief Understand of self test and fault diagnosis concept
- To Implementation of ALU in FPGA
- To Familiarize with ASIC design concept

LIST OF EXPERIMENTS:

1.	Analysis of Asynchronous and clocked synchronous sequential circuits
2.	Built in self test and fault diagnosis
3.	Sensor design using simulation tools
4.	Design, simulation and analysis of signal integrity
5.	Design and Implementation of ALU in FPGA using VHDL and Verilog
6.	Modeling of Sequential Digital system using Verilog and VHDL

7.	Flash controller programming - data flash with erase, verify and fusing
8.	System design using ASIC
	TOTAL : 60 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Design sensor using simulation tools.
2.	Explain built in self test and fault diagnosis.
3.	Explain design, simulation and analysis of signal integrity
4.	Demonstrate design of ALU in FPGA using VHDL and Verilog
5.	Assess flash controller programming - data flash with erase, verify and fusing

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	-	-	3	-	2	2	1	2
CO2	2	2	2	2	2	3	-	-	3	-	2	2	2	2
CO3	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO4	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO5	2	2	2	3	3	3	-	-	3	-	2	3	3	2
18AEPC11	2	2	2	3	3	3	-	-	3	-	2	3	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

SEMESTER III

18AEPC13	ELECTRONIC PRODUCT DESIGN AND DEVELOPMENT	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the product design and development
- To be familiar in PCB and PCB design
- To understand hardware and software testing methods

UNIT I	PRODUCT DESIGN AND DEVELOPMENT	9

Introduction, Product development basics, Product development stages, Identification of the customer requirements, Designing the product ,Techno-commercial feasibility of a product, Pilot production batch, Product assessment, Availability, Screening test of component, redundancy, Effects of environmental conditions on reliability, Comparison between repairable and non-repairable systems, Failure rates of electronic components, Ergonomic and aesthetic design considerations.

UNIT II	FUNDAMENTALS OF PCB AND PCB DESIGN	9

Introduction to PCBs, Layout, Issues related to PCB size, Interconnection parameters, Recommendations for Power and ground traces routing, PCB design for digital circuits, Noise due to ground and supply line, Grounds, Returns and Shields, PCB design rules for analog circuits, Design issues related to supply and ground conductors, Multilayer Boards, Component assembly techniques, Testing of assembled PCBs, Board layout checklist, Bare board testing, Testing of multilayer PCB, Compare of PCBs.

UNIT III	MODERN PCB DESIGN	9

Introduction, Computer-aided design, Automation in design, Soldering techniques, Soldering testing, Packages for semiconductor devices and ICs, Reliability issues in ICs, Parastic elements, High-speed PCBs and parasitic elements, PCB designing for microprocessor-based circuits, High speed PCB design, Design consideration in high speed PCBs, Component mounting under vibration ,SMDs, Cable.

UNIT IV	HARDWARE, SOFTWARE DESIGN AND TESTING METHODS	9
Introduction, Logic analyzer, uses of logic analyze, Oscilloscope Probes, Signal integrity, Use and limitation of Different types of analysis, SPICE, Monte-Carlo analysis, evolution of virtual instrumentation. Introduction, Phases of software design, Goals of software design, Design of Structured program, Testing and debugging of program, Algorithmic state machine, Finite state machines, Selection of language for software development, Assemblers, Compilers, Simulators, Emulators.		
UNIT V	**ELECTRONIC PRODUCT TESTING**	**9**
Introduction, Environmental testing, Temperature testing, Thermal modelling of components, Humidity testing, Electrical overstress testing, Altitude testing, Special testing, Environmental test chambers and rooms, Various test on enclosures, EMI and EMC related testing, EMC and Compliance, Conducted emission test using time domain principle, Radiated emission test, Importance of standards, Standards and Standard developing organisations, List of some standards, CE marking and certification, UL marking and certification, IEC standards, IEC safety standards: CAT standards.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Design electronic products
2.	Apply fundamentals of PCB and PCB design
3.	Implement and Test hardware design
4.	Model Software design and testing
5.	Prepare product documentation

REFERENCES:	
1.	*R.G.Kaduskar,V.B.Baru,Electronic Product design, second edition*
2.	*Bert Haskell, Portable Electronics Product design and development*
3.	*Horowitz, The Art of Electronics*
4.	*https://www.amazon.com/Electronic-Product-Design-V-B-Kaduskar-ebook/dp/B01LZF18QV*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	3	-	-	-	-	-	2	-	-	2	2	-
CO2	3	3	2	-	-	-	-	-	3	-	-	3	3	-
CO3	2	2	2	-	-	-	-	-	1	-	2	3	2	-
CO4	2	3	2	2	-	2	-	-	2	-	-	3	2	-
CO5	3	2	2	-	-	-	-	-	2	-	-	3	2	-
	2	3	2	1	-	1	-	-	2	-	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPC14	**ELECTRONIC PRODUCT DESIGN LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

Objectives:

- To understand the process of electronic product design
- To be familiar in PCB and PCB design
- To be familiar in designing of interfaces

LIST OF EXPERIMENTS:

1.	Design template , PCB, assemble components and verify the working of Regulated Power supplies
2.	Design template , PCB, assemble components and verify the working of Inverter / UPS
3.	Design template , PCB, assemble components and verify the working of Function Generator
4.	Design template , PCB, assemble components and verify the working of PAM/PWM/PPM Modulator / Demodulator
5.	Design template , PCB, assemble components and verify the working of AM/FM Generator / Receiver
6.	Design template , PCB, assemble components and verify the working of Audio/Video Amplifier

7.	Design template , PCB, assemble components and verify the working of Computer interfaces
8.	Design template , PCB, assemble components and verify the working of Microcontroller / Microprocessor interfaces
9.	Design template , PCB, assemble components and verify the working of RF circuits
	TOTAL : 60 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Design of power supplies and Inverter/UPS
2.	Design of different modulators
3.	Design of transmitter and receiver
4.	Design of different interfaces
5.	Analyze the working of audio/video amplifiers

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	3	-	-	-	-	-	2	-	-	2	2	-
CO2	3	3	2	-	-	-	-	-	3	-	-	3	3	-
CO3	2	2	2	-	-	-	-	-	1	-	2	3	2	-
CO4	2	3	2	2	-	2	-	-	2	-	-	3	2	-
CO5	3	2	2	-	-	-	-	-	2	-	-	3	2	-
	2	3	2	1	-	1	-	-	2	-	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

PROFESSIONAL ELECTIVES (PE)

18AEPE01	DIGITAL CONTROL ENGINEERING	L	T	P	C
		2	1	0	3

OBJECTIVES:

- To learn the principles of PI,PD,PID controllers
- To analyse time and frequency response of discrete time control system
- To be familiar in digital control algorithms.

UNIT I	CONTROLLERS IN FEEDBACK SYSTEMS	6+3

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

UNIT II	BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS	6+3

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction

UNIT III	MODELING OF SAMPLED DATA CONTROL SYSTEM	6+3

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV	DESIGN OF DIGITAL CONTROL ALGORITHMS	6+3

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V	PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS	6+3

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

	TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Describe continuous time and discrete time controllers analytically.
2.	Define and state basic analog to digital and digital to analog conversion principles.
3.	Analyze sampled data control system in time and frequency domains.
4.	Design simple PI, PD, PID continuous and digital controllers.
5.	Develop schemes for practical implementation of temperature and motor control systems.

REFERENCES:	
1.	*John J. D'Azzo, "ConstantiveHoupios, Linear Control System Analysis and Design", Mc Graw Hill,1995*
2.	*Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.*
3.	*M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	-	-	-	-	-	-	3	-	3	2	-
CO2	2	3	2	-	-	-	-	-	-	2	-	3	2	-
CO3	3	2	2	-	-	2	-	-	-	1	1	3	2	-
CO4	3	3	2	-	-	2	-	-	-	2	-	3	2	-
CO5	2	2	2	-	-	-	-	-	-	2	-	3	2	-
18AEPE01	3	3	2	-	-	2	-	-	-	2	1	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE02	COMPUTER ARCHITECTURE	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the difference between pipeline and parallel processing concepts
- To study various types of processor architectures and the importance of scalable architectures
- To study Memory Optimization and Technique.

UNIT I	COMPUTER DESIGN AND PERFORMANCE MEASURES	9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi- vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures

UNIT II	PARALLEL PROCESSING, PIPELINING AND ILP	9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III	MEMORY HIERARCHY DESIGN	9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV	MULTIPROCESSORS	9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V	MULTI-CORE ARCHITECTURES	9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

	TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to

1.	Discuss about different architectures .
2.	Explain parallel processing and pipelining.
3.	Explain design of memory hierarchies.
4.	Assess Performance Issues and Synchronization issues.
5.	Compare multicore architectures.

REFERENCES:

1.	*David E. Culler, Jaswinder Pal Singh, "Parallel Computing Architecture: A hardware/ software approach", Morgan Kaufmann / Elsevier, 1997.*
2.	*Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012.*
3.	*Hwang Briggs, "Computer Architecture and parallel processing", McGraw Hill, 1984.*
4.	*John L. Hennessey and David A. Patterson, "Computer Architecture – A quantitative approach", Morgan Kaufmann / Elsevier, 4th. edition, 2007.*
5.	*John P. Hayes, "Computer Architecture and Organization", McGraw Hill*
6.	*John P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003.*
7.	*Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.*
8.	*William Stallings, "Computer Organization and Architecture – Designing for Performance", Pearson Education, Seventh Edition, 2006.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	-	-	-	-	-	-	3	-	2	2	-
CO2	2	3	1	1	-	-	-	-	-	2	-	2	2	-
CO3	2	2	1	-	-	2	-	-	-	1	1	2	2	-
CO4	2	3	2	1	-	2	1	-	-	2	-	2	2	-
CO5	2	2	2	-	-	-	-	-	-	2	-	2	2	-
18AEPE02	2	3	2	-	-	2	-	-	-	2	1	2	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE03	DIGITAL VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the principles of MOS transistor and CMOS inverter.
- To study the various latches and registers, layout and stick diagram of digital circuits.
- To gain knowledge about different building blocks and architecture.

UNIT I	MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II	COMBINATIONAL LOGIC CIRCUITS	9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore‟s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III	SEQUENTIAL LOGIC CIRCUITS	9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV	ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES	9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V	INTERCONNECT AND CLOCKING STRATEGIES	9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL : 45 PERIODS

OUTCOMES: Upon completion the course , the students will have the ability to

1.	Design digital systems using MOS transistor and invertors.
2.	Understand layout, stick diagram in combinational logic circuits

3.	Discuss various latches and registers in sequential circuits.
4.	Discuss design methodology of arithmetic building block.
5.	Analyze tradeoffs of the various circuit choices for each of the building blocks.

REFERENCES:

1.	*Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.*
2.	*N.Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addison Wesley, 1993.*
3.	*Jacob Baker, "CMOS: Circuit Design, Layout, and Simulation", Third Edition Wiley IEEE Press 2010.*
4.	*Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.*
5.	*M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	_	_	_	_	_	2	_	2	3	3	_
CO2	3	3	2	_	_	_	_	_	2	_	2	2	2	_
CO3	3	2	2	_	_	_	_	_	2	_	2	2	2	_
CO4	3	3	2	_	_	_	_	_	2	_	2	3	3	_
CO5	3	2	2	_	_	_	_	_	2	_	2	2	2	_
18AEPE03	3	3	2	_	_	_	_	_	2	_	2	2	2	_

1-Low 2—Moderate (Medium) 3-High

18AEPE04	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the basics of EMI
- Be familiar with EMI sources and problems.
- To understand about EMI/EMC standards.

UNIT I	BASIC THEORY	9

Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II	COUPLING MECHANISM	9

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III	EMI MITIGATION TECHNIQUES	9

Working principle of Shielding and Murphy‟s Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV	STANDARD AND REGULATION	9

Need for Standards, Generic/General Standards for Residential and Industrial environment, Basic Standards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

UNIT V	EMI TEST METHODS AND INSTRUMENTATION	9

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian

STD test methods.	
	TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Define sources and hazards of EMI and EMC.
2.	Compare different coupling mechanisms.
3.	Identify Standards.
4.	Compare EMI test methods.
5.	Discuss EMI mitigation techniques.

REFERENCES:	
1.	*Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.*
2.	*Clayton Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience, 2006.*
3.	*Daryl Gerke and William Kimmel, "EDN"s Designer"s Guide to Electromagnetic Compatibility", Elsevier Science & Technology Books, 2002.*
4.	*Dr Kenneth L Kaiser, "The Electromagnetic Compatibility Handbook", CRC Press 2005.*
5.	*Electromagnetic Compatibility by Norman Violette ,Published by Springer, 2013.*
6.	*Electromagnetic Interference and Compatibility: Electrical noise and EMI specifications Volume 1 of A Handbook Series on Electromagnetic Interference and Compatibility, Donald R. J. White Publisher-Don white consultants Original from the University of Michigan Digitized 6 Dec 2007.*
7.	*Henry W. Ott, "Electromagnetic Compatibility Engineering", John Wiley & Sons Inc, Newyork, 2009.*
8.	*V Prasad Kodali, "Engineering Electromagnetic Compatibility", IEEE Press, Newyork, 2001.*
9.	*W Scott Bennett, "Control and Measurement of Unintentional Electromagnetic Radiation", John Wiley & Sons Inc., (Wiley Interscience Series) 1997.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	-	1	-	1	-	-	-	2	-	-	1	2	2
CO2	2	-	1	1	-	-	-	-	2	-	-	1	2	2
CO3	3	-	1	1	-	-	-	-	2	1	-	-	-	1
CO4	2	-	1	1	-	-	-	-	2	-	-	-	-	-
CO5	3	-	1	-	-	-	-	-	2	1	-	1	2	2
18AEPE04	2	-	1	1	-	-	-	-	2	-	-	1	2	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE05	**CAD FOR VLSI**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To learn VLSI Design methodologies and understand the concepts behind the VLSI design rules and routing techniques
- To study the simulation techniques at various levels in VLSI design flow
- To understand the concepts of various algorithms used for floor planning and routing techniques.

UNIT I	**INTRODUCTION TO VLSI DESIGN FLOW**	**9**

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II	**LAYOUT, PLACEMENT AND PARTITIONING**	**9**

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III	FLOOR PLANNING AND ROUTING	9
Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing		
UNIT IV	**SIMULATION AND LOGIC SYNTHESIS**	**9**
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.		
UNIT V	**HIGH LEVEL SYNTHESIS**	**9**
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Discuss the VLSI automation tools and design methodologies.
2.	Analyze the various placement algorithms.
3.	Analyze the concepts of floor planning and routing.
4.	Use the simulation techniques at various levels in VLSI design flow.
5.	Outline the hardware models for high level synthesis.

REFERENCES:

1.	*S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.*
2.	*N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.*
3.	*Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World scientific 1999.*
4.	*Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.*
5.	*Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	_	3	1	3	2	2	3	3	2
CO2	3	3	2	3	1	_	2	1	2	1	2	2	2	2
CO3	3	3	2	3	1	_	2	1	2	1	2	2	2	2
CO4	3	2	2	2	3	_	3	1	3	2	2	3	3	2
CO5	3	2	2	2	2	_	2	1	2	1	2	2	2	2
18AEPE05	3	3	2	2	3	_	2	1	2	1	2	2	2	2

1-Low 2—Moderate (Medium) 3-High

18AEPE06	**NANOELECTRONICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To learn and understand basic concepts of Nano electronics.
- To know about electronic and photonic materials.
- To understand how transistor as Nano device.

UNIT I	**SEMICONDUCTOR NANO DEVICES**	**9**

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II	**ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS**	**9**

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III	THERMAL SENSORS	9
Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.		
UNIT IV	**GAS SENSOR MATERIALS**	**9**
Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.		
UNIT V	**BIOSENSORS**	**9**
Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	understand the operation of micro devices, micro systems and their applications
2.	design the micro devices, micro systems using the MEMS fabrication process.
3.	Gain a knowledge of basic approaches for various sensor design
4.	Gain a knowledge of basic approaches for various actuator design
5.	Develop experience on micro/nano systems for photonics .

REFERENCES:	
1.	*K.E. Drexler, "Nano systems", Wiley,1992.*
2.	*M.C. Petty, "Introduction to Molecular Electronics", 1995.*
3.	*W. Ranier, "Nano Electronics and Information Technology", Wiley, 2003.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	-	-	-	-	-	-	-	3	-	3	2	-
CO2	3	-	-	-	-	-	-	-	-	2	-	3	2	-
CO3	2	2	-	-	-	2	-	-	-	1	1	3	2	-
CO4	2	2	-	-	2	2	-	-	-	2	-	3	2	-
CO5	2	1	-	3	1	-	-	-	-	2	-	3	2	-
18AEPE06	3	2	-	2	1	2	-	-	-	2	1	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE07	**SENSORS AND SIGNAL CONDITIONING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- study about the various types of sensors
- study different types of actuators and their usage.

UNIT I	**SENSOR CHARACTERISTICS**	**9**

sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II	**RESISTIVE AND REACTIVE SENSORS**	**9**

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

UNIT III	SELF-GENERATING SENSORS	9
Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.		
UNIT IV	**ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS**	**9**
Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.		
UNIT V	**DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS**	**9**
Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions,		
magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Discuss the characteristics of Sensors
2.	Discuss Resistive and Reactive sensors
3.	Discuss Self-generating sensors.
4.	Compare Actuators.
5.	Evaluate digital sensors and semiconductor device sensors.

REFERENCES:

1.	*Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2006.*
2.	*D. Johnson, "Process Control Instrumentation Technology", John Wiley and Sons.*
3.	*D.Patranabis, "Sensors and Transducers", TMH 2003.*
4.	*E.O. Doeblin, "Measurement System : Applications and Design", McGraw Hill publications.*
5.	*Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	1	1	3	1	2	2	1	2
CO2	2	2	2	2	2	3	1	1	3	1	2	2	2	2
CO3	2	2	2	3	3	3	1	1	3	1	2	3	3	2
CO4	2	2	2	3	3	3	1	1	3	1	2	3	3	2
CO5	2	2	2	3	3	3	1	1	3	1	2	3	3	2
18AEPE07	2	2	2	3	3	3	1	1	3	1	2	3	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE08	**MEMS AND NEMS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To introduce the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.

UNIT I	**OVERVIEW**	**9**

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II	**MEMS FABRICATION TECHNOLOGIES**	**9**

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III	MICRO SENSORS	9
MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.		
UNIT IV	**MICRO ACTUATORS**	**9**
Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators. components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis		
UNIT V	**NANOSYSTEMS AND QUANTUM MECHANICS**	**9**
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	understand the operation of micro devices, micro systems and their applications.
2.	design the micro devices, micro systems using the MEMS fabrication process.
3.	Gain a knowledge of basic approaches for various sensor design.
4.	Gain a knowledge of basic approaches for various actuator design.
5.	Develop experience on micro/Nano systems for photonics.

REFERENCES:

1.	*Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.*
2.	*Marc Madou, "Fundamentals of Microfabrication", CRC press 1997*
3.	*Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001*
4.	*Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.*
5.	*Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata McGraw Hill, 2002*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	-	-	-	2	2	-	3	2	3	-	3	2	-
CO2	2	2	2	-	2	-	3	-	-	-	-	3	2	-
CO3	2	3	-	2	-	2	-	-	-	-	3	3	2	-
CO4	2	3	2	-	-	-	2	2	-	2	-	3	2	-
CO5	-	2	2	-	3	2	-	2	2	-	2	3	2	-
18AEPE08	-	-	-	2	3	3	-	-	2	-	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE09	**DSP PROCESSORS ARCHITECTURE AND PROGRAMMING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To learn about basics of DSP processors
- To know about the internal architectures of advanced DSP processors
- To become familiar with programming techniques

UNIT I	**FUNDAMENTALS OF PROGRAMMABLE DSPs**	**9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II	**SPECIAL FUNCTIONS**	**9**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals

UNIT III	**LINEAR PROGRAMMING**	**9**

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.		
UNIT IV	**LINEAR PROGRAMMING**	**9**
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.		
UNIT V	**ALGEBRAIC EQUATIONS**	**9**
Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Understand various modules in the DSP processor
2.	Understand the special functions of DSP processors
3.	Demonstrate various programming techniques
4.	Demonstrate Digital Signal processing technique
5.	Design DSP based System.

REFERENCES:	
1.	*Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012.*
2.	*B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.*
3.	*RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A JOHN WILEY & SONS, INC., PUBLICATION, 2005*
4.	*User guides Texas Instrumentation, Analog Devices, Motorola.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	-	-	-	1	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	1	-	-	-	-	-	-	-	-	-
CO3	3	1	-	-	-	-	-	-	-	-	-	-	3	-
CO4	2	2	2	-	3	-	2	2	2	-	-	3	3	1
CO5	1	-	2	2	2	-	3	2	1	-	-	3	3	1
18AEPE09	3	-	1	-	1	-	-	1	-	-	-	1	3	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE10	RF SYSTEM DESIGN	L	T	P	C
		2	1	0	3

OBJECTIVES:

- To introduce the principles of operation and design principles associated with the important blocks of RF Front end.
- To design RF amplifier, oscillators and mixers.
- To study about the characteristics of PLL and frequency synthesizers.

UNIT I	CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS ANDARCHITECTURES	6+3

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II	IMPEDANCE MATCHING AND AMPLIFIERS	6+3

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III	FEEDBACK SYSTEMS AND POWER AMPLIFIERS	6+3
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.		
UNIT IV	**MIXERS AND OSCILLATORS**	**6+3**
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.		
UNIT V	**PLL AND FREQUENCY SYNTHESIZERS**	**6+3**
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Define various transceiver specifications and compare different transceivers.
2.	Design impedance matching networks for different amplifiers.
3.	Analyze the stability of feedback systems
4.	Discuss different types of mixers and oscillators
5.	Explain different phase locked loops and frequency synthesizers.

REFERENCES:

1.	*B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001*
2.	*B.Razavi, "RF Microelectronics", Pearson Education, 1997.*
3.	*Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.*
4.	*Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/*
5.	*T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	1	-	1	2	-	-	-	2	-	-	1	1	2
CO2	3	1	-	2	2	-	-	1	2	-	-	1	2	2
CO3	2	1	-	1	2	-	-	1	1	-	-	1	2	2
CO4	2	1	-	2	3	-	-	-	-	-	-	-	1	-
CO5	2	1	-	1	2	-	-	1	2	-	-	-	1	1
18AEPE10	2	1	-	1	2	-	-	1	2	-	-	1	1	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE11	**SPEECH SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		2	**1**	**0**	**3**

OBJECTIVES:

- To study basic concepts of processing speech signals.
- To study time and frequency domain speech processing methods
- To understand predictive analysis of speech.

UNIT I	**MECHANICS OF SPEECH AND AUDIO**	**6+3**

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II	TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS	6+3
Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies		
UNIT III	**AUDIO CODING AND TRANSFORM CODERS**	**6+3**
Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder – Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding – Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization - MDCT with Vector Quantization.		
UNIT IV	**TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING**	**6+3**
Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – HomomorphicVocoders.		
UNIT V	**PREDICTIVE ANALYSIS OF SPEECH**	**6+3**
Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin‟s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Discuss mechanics of Speech and Audio.
2.	Discuss various M-band filter-banks for audio coding
3.	Evaluate audio coding and transform coders
4.	Discuss time and frequency domain methods for speech processing

5.	Explain predictive analysis of speech

REFERENCES:	

1.	*B.Gold and N.Morgan, "Speech and Audio Signal Processing", Wiley and Sons, 2000.*
2.	*L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech Signals", Prentice Hall, 1978.*
3.	*Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio And Acoustics, Academic Publishers*
4.	*UdoZölzer, "Digital Audio Signal Processing", Second Edition A John Wiley& sons Ltd*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	1	1	3	1	2	2	1	2
CO2	2	2	2	2	2	3	1	1	3	1	2	2	2	2
CO3	2	2	2	3	3	3	1	1	3	1	2	3	3	2
CO4	2	2	2	3	3	3	1	1	3	1	2	3	3	2
CO5	2	2	2	3	3	3	1	1	3	1	2	3	3	2
18AEPE11	2	2	2	3	3	3	1	1	3	1	2	3	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE12	SOLID STATE DEVICE MODELLING AND SIMULATION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study physics of MOSFET devices.
- To understand the concept of device modelling.
- To study mathematical techniques of device simulations.

UNIT I	MOSFET DEVICE PHYSICS MOSFET	9

capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II	DEVICE MODELLING	9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III	MULTISTEP METHODS	9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV	MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS	9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V	SIMULATION OF DEVICES	9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Explain the importance of MOS Capacitor and Small signal modelling

2.	Apply and determine the drift diffusion equation and stiff system equation.
3.	Offer clues to qualitative understanding of the physics of a new device and conversion of this understanding into equations.
4.	Model the MOS transistor using schrodinger equation and Multistep methods.
5.	Explain how the equations get lengthy and parameters increase in number while developing a compact model.

REFERENCES:

1.	*Arora, N., "MOSFET Modeling for VLSI Simulation", Cadence Design Systems, 2007*
2.	*Chua, L.O. and Lin, P.M., "Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques", Prentice-Hall., 1975*
3.	*Fjeldly, T., Yetterdal, T. and Shur, M., "Introduction to Device Modeling and Circuit Simulation", Wiley-Interscience., 1997*
4.	*Grasser, T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company., 2003*
5.	*Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag.,1984*
6.	*Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO2	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO3	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO4	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO5	3	3	3	3	3	2	2	-	-	3	-	2	3	2
18AEPE12	3	3	3	3	3	2	2	-	-	3	-	2	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE13	ADVANCED MICROPROCESSOR AND MICROCONTROLLER ARCHITECTURES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To familiarize about the features, specification and features of modern microprocessors.
- To gain knowledge about the architecture of 32 and 64 bit microprocessors and microcontrollers salient features associated with them.
- To study interfacing of microprocessor/microcontroller with the external peripheral.

UNIT I	FEATURES OF MODERN MICROPROCESSORS	9

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over clocking – integrated graphics processing - performance benchmarks.

UNIT II	HIGH PERFORMANCE CISC ARCHITECTURES	9

Introduction to IA 32 bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT III	HIGH PERFORMANCE RISC ARCHITECTURE – ARM	9

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3-stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles)

UNIT IV	FEATURES OF MODERN MICROCONTROLLER	9

Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces– Communication interfaces (SPI,I2C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces .

UNIT V	HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES	9

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-

M3 architecture	
	TOTAL : 45 PERIODS
COURSE OUTCOMES:	Upon completion the course , the students will have the ability
1.	To explain the features and important specifications of modern microprocessors.
2.	To explain the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures.
3.	To explain the salient features RISC processors based on ARM architecture and different application profiles of ARM core .
4.	To explain the features and important specifications of modern microcontrollers.
5.	To explain about ARM – M3 architecture and its salient features
REFERENCES:	
1.	*Barry. B. Breg," The Intel Microprocessors" , PHI,2008.*
2.	*Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.*
3.	*Intel Inc, "Intel 64 and IA-32 Architectures Developer"s Manual", Volume-I, 2016*
4.	*Joseph Yiu, "The Definitive Guide to the ARM ® Cortex-M3", Newnes, 2010.*
5.	*Scott Mueller, "Upgrading and Repairing PCs", 20th edition, Que.*
6.	*Steve Furber, ," ARM System –On –Chip architecture "Addision Wesley , 2000.*
7.	*Trevor Martin, "The Designer"s Guide to the Cortex-M Processor Family", Newnes, 2013.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	2	-	-	3	-	2	2	2	3
CO2	3	2	2	2	-	3	-	-	3	-	2	2	2	3
CO3	3	2	2	2	-	3	-	-	3	-	2	3	2	3
CO4	3	2	2	2	-	3	-	-	3	-	2	3	2	3
CO5	3	2	2	2	-	3	-	-	3	-	2	3	2	3
18AEPE13	3	2	2	2	-	3	-	-	3	-	2	3	2	3

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE14	SYSTEM ON CHIP	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand what SOC is and what the difference between SOC and Embedded system.
- To cover the basics of SOC design, hardware software co design and synthesis.
- To study different levels of SOC verification.

UNIT I	INTRODUCTION	9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

UNIT II	SYSTEM LEVEL MODELLING	9

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III	HARDWARE AND SOFTWARE CO -DESIGN	9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV	SYNTHESIS	9

System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling.

UNIT V	SOC VERIFICATION AND TESTING	9

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism

	TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	acquire knowledge about Top-down SoC design flow
2.	apply knowledge about Front-end and back-end chip design
3.	model designing communication Networks
4.	Understand hardware, software and interface synthesis
5.	interpret the design methodologies for SoC

REFERENCES:	
1.	*D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.*
2.	*D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009*
3.	*Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.*
4.	*Jan Ho¨ ller, VlasiosTsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.*
5.	*Olivier Hersent, David Boswarthick, Omar Elloumi , "The Internet of Things – Key applications and Protocols", Wiley, 2012*
6.	*Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoCdesing",CRC press, 2008.*
7.	*M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005*
8.	*M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994*
9.	*P. Marwedel, Embedded System Design, Springer, 2003. G. De Micheli, Synthesis and Optimization of Digital Circuits*
10.	*Prakash Rashinkar, Peter Paterson and Leena Singh, System-on-a chip verification: Methodology and techniques, kluwer Academic Publishers 2002*
11.	*T. Noergaard, Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers, Newnes*
12.	*Vijay K. MadisettiChonlamethArpikanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2005.*
13.	*Youn-Long Steve Lin, Essential Issues in SOC Design Designing Complex Systems-on-Chip, Springer, 2006*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	-	-	-	-	-	-	-	-	3	2	-
CO2	3	2	-	-	-	-	-	1	-	-	-	3	2	-
CO3	2	1	-	-	-	-	-	-	-	-	1	3	2	-
CO4	3	2	1	-	1	2	1	1	-	-	-	3	2	-
CO5	1	2	2	-	1	1	2	-	-	-	-	3	2	-
18AEPE14	3	2	1	-	2	2	1	2	-	-	1	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE15	**ROBOTICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics.
- To understand mobile robot localization.
- To understand robot planning and navigation.

UNIT I	**LOCOMOTION AND KINEMATICS**	**9**

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT II	**ROBOT PERCEPTION**	**9**

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data

UNIT III	MOBILE ROBOT LOCALIZATION	9
Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments		
UNIT IV	**MOBILE ROBOT MAPPING**	**9**
Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM – extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fast SLAM algorithm.		
UNIT V	**PLANNING AND NAVIGATION**	**9**
Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Define robot locomotion, kinematics models and constraints
2.	Understand different types of robot localization techniques
3.	Implement robot mapping techniques
4.	Understand planning and navigation in robotics
5.	Build and analyse the obstacle avoidance robot

REFERENCES:

1.	*Gregory DudekandMichael Jenkin, "Computational Principles of Mobile Robotics", Second Edition, Cambridge University Press, 2010.*
2.	*Howie Choset et al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", A Bradford Book, 2005.*
3.	*Maja J. Mataric, "The Robotics Primer", MIT Press, 2007.*
4.	*Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, "Introduction to autonomous mobile robots", Second Edition, MIT Press, 2011.*
5.	*Sebastian Thrun, Wolfram Burgard, and Dieter Fox, "Probabilistic Robotics", MIT Press, 2005.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	2	-	-	-	-	-		-	-	-
CO3	-	3	-	-	3	-	2	-	-	-	-	-	-	2
CO4	2	2	-	-	3	-	3	-	-	-	-	2	-	-
CO5	2	-	2	-	3	-	3	-	2	-	-	3	3	3

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE16	**PHYSICAL DESIGN OF VLSI CIRCUITS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To introduce the physical design concepts such as layout rules, circuit abstraction, layout methodologies and packaging.
- To study placement of design using top down approach.
- To study the performance of circuits layout designs, compaction techniques.

UNIT I	**INTRODUCTION TO VLSI TECHNOLOGY**	**9**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms

UNIT II	**PLACEMENT USING TOP-DOWN APPROACH**	**9**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III	ROUTING USING TOP DOWN APPROACH	9
Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs		
UNIT IV	**PERFORMANCE ISSUES IN CIRCUIT LAYOUT**	**9**
Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization		
UNIT V	**SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION**	**9**
Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Understand different gate arrays in VLSI.
2.	Analyze different placement methods.
3.	Explain different types of routing
4.	Discuss performance issues in circuit layout
5.	Outline 1D compaction- 2D compaction.

REFERENCES:

1.	*Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.*
2.	*Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill Int. Edition 1995*
3.	*N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.*
4.	*Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World scientific 1999.*
5.	*Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.*

COURSE ARTICULATION MATRIX:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PSO 1	PSO 2	PSO 3
CO1	3	1	1	2	_	_	2	_	2	2	2	1	1	2
CO2	3	2	2	3	_	_	2	_	2	1	2	2	2	2
CO3	3	1	1	2	_	_	2	_	2	2	2	1	1	2
CO4	3	1	1	1	_	_	2	_	2	2	2	1	1	2
CO5	2	1	1	2	_	_	1	_	2	2	2	1	1	2
18AEPE16	3	2	1	2	_	_	2	_	2	2	2	1	1	2

1-Low 2—Moderate (Medium) 3-High

18AEPE17	**HIGH PERFORMANCE NETWORKS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networks.
- To study the types of VPN and tunnelling protocols for security.
- To discuss traffic modelling.

UNIT I	**INTRODUCTION**	**9**

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.

UNIT II	**MULTIMEDIA NETWORKING APPLICATIONS**	**9**

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III	**ADVANCED NETWORKS CONCEPTS**	**9**

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS-operation, Routing, Tunneling and use of FEC, Traffic Engineering, and MPLS based VPN, overlay networks- P2P connections.

UNIT IV	TRAFFIC MODELLING	9
Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.		
UNIT V	**NETWORK SECURITY AND MANAGEMENT**	**9**
Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Discuss about different communication network technologies
2.	Explain different protocols and services for multimedia applications
3.	Describe VPN concepts and services
4.	Analyze traffic of networks with mathematical techniques
5.	Discuss about network security and attacks.

REFERENCES:	
1.	*Aunurag Kumar, D. M Anjunath, Joy Kuri, "Communication Networking", Morgan Kaufmann Publishers, 1st edition 2004.*
2.	*Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet", fifth edition, Pearson education 2006*
3.	*Hersent Gurle & Petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003*
4.	*J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003*
5.	*Larry l.Peterson & Bruce S.David, "Computer Networks: A System Approach"- 1996*
6.	*LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.*
7.	*Nader F.Mir ,Computer and Communication Networks, first edition 2010*
8.	*Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	1	-	-	2	2	2	-	-	2	1	1
CO2	2	2	1	1	-	-	2	2	-	-	-	2	1	-
CO3	3	2	-	1	-	-	1	2	2	-	-	2	-	-
CO4	3	3	1	3	-	-	2	3	-	-	-	-	-	1
CO5	2	2	-	2	-	-	2	2	-	-	-	-	-	-
18AEPE17	3	2	-	1	-	-	2	2	-	-	-	2	-	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE18	**PATTERN RECOGNITION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To learn about supervised and unsupervised pattern classifiers
- To learn about different clustering methods.
- To familiarize about different feature extraction techniques
- To explore the role of Hidden Marko model and SVM in pattern recognition
- To understand the application of Fuzzy logic and genetic algorithms for pattern classifier

UNIT I	**PATTERN CLASSIFIER**	**9**

Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT II	**CLUSTERING**	**9**

Clustering for unsupervised learning and classification–Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III	FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION	9
Principle component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation – Elements of formal grammars, Syntactic description – Stochastic grammars – Structural Representation.		
UNIT IV	**HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE**	**9**
State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection.		
UNIT V	**RECENT ADVANCES**	**9**
Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Differentiate between supervised and unsupervised classifiers
2.	Analyze different clustering methods.
3.	Classify the data and identify the patterns.
4.	Extract feature set and select the features from given data set.
5.	Apply fuzzy logic and genetic algorithms for classification problems

REFERENCES:

1.	*Andrew Webb, "Stastical Pattern Recognition", Arnold publishers, London,1999*
2.	*C.M.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.*
3.	*M. Narasimha Murthy and V. Susheela Devi, "Pattern Recognition", Springer 2011.*
4.	*Menahem Friedman , Abraham Kandel, "Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches", World Scientific publishing Co. Ltd, 2000.*
5.	*Robert J.Schalkoff, "Pattern Recognition Statistical, Structural and Neural Approaches", John Wiley & Sons Inc., New York, 1992.*
6.	*R.O.Duda, P.E.Hart and D.G.Stork, "Pattern Classification", John Wiley, 2001*
7.	*S.Theodoridis and K.Koutroumbas, "Pattern Recognition", 4th Ed., Academic Press. 2009.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	3	1	2	1	2	2	2	3	2	1	1
CO2	2	2	1	3	1	2	1	2	1	1	2	1	1	-
CO3	3	2	2	1	2	1	-	1	2	-	-	2	1	-
CO4	3	3	1	2	2	1	-	2	-	2	2	1	1	1
CO5	2	2	1	2	-	-	2	1	1	-	1	2	2	1
18AEPE17	3	2	2	1	1	2	2	2	1	-	1	2	1	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE19	**SECURE COMPUTING SYSTEMS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To learn different computer security mechanism and management techniques.
- To gain knowledge about computer hardware security.
- To apply programming knowledge in hardware.

UNIT I	**COMPUTER SECURITY AND MANAGEMENT**	**9**

Overview of Computer Security, Threats, Malware, Vulnerabilities, Authentication, Access Control, Security Management Models, Security Management Practices, Protection Mechanisms, Legal aspects of security, Ethical Hacking.

UNIT II	**HARDWARE SECURITY**	**9**

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Countermeasures of Side Channel Attack, Secure Hardware Intellectual Properties, Physically Unclonable Functions(PUFs), Secure PUF.

UNIT III	ASSEMBLY AND OPERATING SYSTEMS SECURITY	9
Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions		
UNIT IV	**ADVANCED COMPUTER ARCHITECTURE**	**9**
Security aspects : Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization		
UNIT V	**NETWORK AND WEBSECURITY**	**9**
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.		
		TOTAL : 45 PERIODS

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Aware of Security aspects
2.	Able to appreciate security in hardware, OS and it future need
3.	Learn security issues in various types of computing networks
4.	The students have firm understanding on basic terminology and concepts related to network and system level security.
5.	Analyze the requirements for a given organizational structure and select the most appropriate networking architecture and technologies.

REFERENCES:	
1.	*Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", Fourth Edition, Pearson Education, 2007*
2.	*Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design Threats and Safeguards", CRC Press, 2015*
3.	*Michael Whitman, Herbert J. Mattord, "Management of Information Security", Third Edition, Course Technology, 2010*
4.	*Shuangbao Wang, Robert S.Ledley, Computer Architecture and Security, Wiley, 2013*
5.	*William Stallings, "Network Security Essentials, Applications and Standards", Dorling Kindersley I P Ltd, Delhi, 2008.*

6.	*Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", Fourth Edition, Pearson Education, 2007*
7.	*Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design Threats and Safeguards", CRC Press, 2015*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	-	-	1	2	-	-	-	-	1	-	2	-
CO2	2	2	2	-	1	2	-	-	2	-	2	-	2	-
CO3	3	1	1	-	3	3	-	-	1	-	2	-	2	-
CO4	3	2	-	-	2	2	-	-	2	-	3	-	2	-
CO5	2	-	2	-	2	3	-	2	2	-	2	-	2	-
18AEPE19	2	2	2	-	2	2	-	-	2	-	2	-	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE20	**SIGNAL INTEGRITY FOR HIGH SPEED DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics
- To learn non-ideal effects of transmission lines.

UNIT I	**SIGNAL PROPAGATION ON TRANSMISSION LINES**	**9**

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II	MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK	9
Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.		
UNIT III	**NON-IDEAL EFFECTS**	**9**
Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors		
UNIT IV	**POWER CONSIDERATIONS AND SYSTEM DESIGN**	**9**
SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis		
UNIT V	**CLOCK DISTRIBUTION AND CLOCK OSCILLATORS**	**9**
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.matrix layout- 1D compaction- 2D compaction.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Understand signal transmission characteristics.
2.	Analyze different signaling methods.
3.	Discuss about various parasitics in transmission lines.
4.	Analyze the power consideration in digital circuits.
5.	Understand clock distribution and clock oscillators.

REFERENCES:

1.	Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003
2.	Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.
3.	*H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.*
4.	*S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.*
5.	*Stephen H. Hall and Howard L.Heck , Advanced Signal Integrity for High-Speed Digital Designs, Wiley-IEEE Press, 2009.*

COURSE ARTICULATION MATRIX:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PSO 1	PSO 2	PSO 3
CO1	3	2	2	2	_	_	2	_	2	2	2	1	1	2
CO2	3	3	3	3	_	_	2	_	2	1	2	2	2	2
CO3	3	2	2	2	_	_	1	_	2	1	2	1	1	2
CO4	3	3	3	3	_	_	2	_	2	1	2	2	2	2
CO5	3	2	2	2	_	_	2	_	1	2	2	1	1	2
18AEPE20	3	2	2	2	_	_	2	_	2	1	2	1	1	2

1-Low 2—Moderate (Medium) 3-High

18AEPE21	**WIRELESS ADHOC AND SENSOR NETWORKS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

- To study the ADHOC networks and its protocols
- To implement the designing of multicast routing and security
- To study the Challenges in QOS and power management schemes

UNIT I	**MAC & TCP IN AD HOC NETWORKS**	**9**

Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT II	**ROUTING IN AD HOC NETWORKS**	**9**

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT III	MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS	9
Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support.		
UNIT IV	**SENSOR MANAGEMENT**	**9**
Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.		
UNIT V	**SECURITY IN AD HOC AND SENSOR NETWORKS**	**9**
Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defence against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability to
1.	Understand the basic concepts of WIRELESS networks and challenges of Ad-hoc and sensor networks.
2.	Classify the design issues and different categories of MAC protocols
3.	Explain the various Ad-hoc routing protocols and transport layer mechanisms
4.	Discuss the sensor characteristics and WSN layer protocols
5.	Illustrate the issues of routing in WSN and QOS related performance measurements

REFERENCES:	
1.	*Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition), World Scientific Publishing, 2011*
2.	*C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.*
3.	*C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2002.*
4.	*ErdalÇayırcı ,Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.*

5.	*Holger Karl, Andreas willig, Protocols and Architectures for Wireless Sensor Networks, John Wiley & Sons, Inc .2005.*
6.	*Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.*
7.	*WaltenegusDargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley and Sons, 2010.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	-	-	-	-	-	-	-	-	3	1	-
CO2	3	3	2	1	-	-	-	-	-	-	-	3	2	-
CO3	3	3	2	1	-	-	-	-	-	-	-	3	2	-
CO4	3	2	-	-	-	-	-	-	-	-	-	3	1	-
CO5	3	3	2	1	1	3	1	-	-	-	-	3	2	2
18AEPE21	3	3	2	1	-	-	-	-	-	-	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEPE22	**HARDWARE - SOFTWARE CO-DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

•	To acquire the knowledge about system specification and modeling.
•	To learn the formulation of partitioning
•	To study the different technical aspects about prototyping and emulation.

UNIT I	**SYSTEM SPECIFICATION AND MODELLING**	**9**

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II	HARDWARE / SOFTWARE PARTITIONING	9
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.		
UNIT III	**HARDWARE / SOFTWARE CO-SYNTHESIS**	**9**
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co- Synthesis Algorithm for Distributed System- Case Studies with any one application.		
UNIT IV	**PROTOTYPING AND EMULATION**	**9**
Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture-Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems		
UNIT V	**DESIGN SPECIFICATION AND VERIFICATION**	**9**
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.		
	TOTAL : 45 PERIODS	

OUTCOMES:	Upon completion the course , the students will have the ability
1.	To understand and to apply design methodologies.
2.	To compare hardware / software co-synthesis.
3.	To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships
4.	To be familiar with modern hardware/software tools for building prototypes.
5.	To demonstrate practical competence in these areas.

REFERENCES:	
1.	*Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design "Kaufmann Publishers,2001.*

2.	*Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.*
3.	*Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	3	2	-	-	-	-	-	-	-	3	2	1
CO2	1	3	2	2	-	-	-	-	-	-	-	3	2	1
CO3	1	2	2	-	-	-	-	-	-	-	1	2	2	1
CO4	3	2	-	-	-	2	-	1	-	-	-	2	2	1
CO5	3	2	3	3	-	2	-	1	-	-	-	3	2	1
18AEPE22	2	2	2	2	-	1	-	1	-	-	-	3	2	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

OPEN ELECTIVES

18AEOE01	INTRODUCTION TO NANOELECTRONICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study semiconductor devices and nano electronics devices
- To study photonic molecular materials and thermal sensors
- To study gas sensor materials and bio sensors

UNIT I	SEMICONDUCTOR NANO DEVICES	9

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II	ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS	9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III	THERMAL SENSORS	9

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV	GAS SENSOR MATERIALS	9

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V	BIOSENSORS	9

Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.	
	TOTAL : 45 PERIODS
OUTCOMES:	Upon completion the course , the students will have the ability to
1.	To be able to understand semiconductor and nano electronic devices
2.	To be able to understand electronic and photonic molecular materials
3.	Ability to understand basic of thermal sensors
4.	Ability to understand gas sensor materials
5.	Ability to understand basic of Bio sensors
REFERENCES:	
1.	*K.E. Drexler, "Nano systems", Wiley,1992.*
2.	*M.C. Petty, "Introduction to Molecular Electronics", 1995.*
3.	*W. Ranier, "Nano Electronics and Information Technology", Wiley, 2003.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	-	3	3	3	1	2	2	-	-	3	2	2	2	3	2
CO2	-	3	3	3	1	2	2	-	-	3	2	2	2	3	2
CO3	-	3	3	3	1	2	2	-	-	3	2	2	2	3	2
CO4	-	3	3	3	1	2	2	-	-	3	2	2	2	3	2
CO5	-	3	3	3	1	2	2	-	-	3	2	2	2	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

18AEOE02	GENETIC ALGORITHMS	L	T	P	C
		3	0	0	3

UNIT I	INTRODUCTION	9
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion		

UNIT II	GENETIC ALGORITHM FOR VLSI	9
GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy -Multiway Partitioning		

UNIT III	HYBRID GENETIC	9
Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.		

UNIT IV	GLOBAL ROUTING	9
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.		

UNIT V	POWER ESTIMATION	9
Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.		

	TOTAL : 45 PERIODS

OUTCOMES	Upon completion the course , the students will have the ability
1.	To apply the basics of Genetic algorithm.
2.	To design genetic algorithm in VLSI.
3.	To describe about hybrid genetic.
4.	To explain about global routing.
5.	To analyse the power estimation in genetic algorithm.

TEXT BOOKS:	

1.	Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2.	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience, 1977.

REFERENCES:	
1.	*Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.*
2.	*John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.*

18AEOE03	**NEURAL NETWORKS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

UNIT I	**INTRODUCTION TO NEURAL NETWORKS**	**9**
Fundamentals of artificial Neural Networks – Biological neurons and their artificial models, Neural processing, learning and Adaptation, Neural Network Learning Rules – Hebbian, Perceptron, delta, widrow – hoff, correlation, winner – take – all, outstar learning rules.		
UNIT II	**PERCEPTRON AND BACK PROPAGATION ALGORITHM**	**9**
Single Layer Perceptions – Multi player Feed forward Networks – Error back propagation training algorithm, problems with back propagation, Boltzmann training, Cauchy training, Combined back propagation / Cauchy training.		
UNIT III	**HOPFIELD MODELS**	**9**
Hopfield networks, Recurrent and Bi-directional Associative Memories, Counter Propagation Network, Artificial Resonance Theory (ART)		
UNIT IV	**APPLICATIONS OF NEURAL NETWORKS**	**9**
Applications of neural networks – Handwritten digit and character recognition, Traveling salesman problem, Neuro controller – inverted pendulum controller		
UNIT V	**EXPERT SYSTEM FOR MEDICAL DIAGONOSIS**	**9**
Applications of neural networks - cerebellar model articulation controller, Robot		

kinematics, Expert systems for Medical Diagnosis.	
	TOTAL : 45 PERIODS
OUTCOMES :	Upon completion the course , the students will have the ability
1.	To obtain the theoretical knowledge about Neural Networks
2.	To understand the concepts of perceptron networks
3.	Acquire the knowledge about the applications of Neural Network in the field of Medical diagnosis

18AEOE04	**MULTIMEDIA COMPRESSION TECHNIQUES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

UNIT I	**MULTIMEDIA COMPONENTS**	**9**
Introduction - Multimedia skills - Multimedia components and their characteristics - Text, sound, images, graphics, animation, video, hardware.		
UNIT II	**AUDIO AND VIDEO COMPRESSION**	**9**
Audio compression–DPCM-Adaptive PCM –adaptive predictive coding-linear Predictive coding-code excited LPC-perpetual coding Video compression –principles-H.261-H.263-MPEG 1, 2, and 4.		
UNIT III	**TEXT AND IMAGE COMPRESSION**	**9**
Compression principles-source encoders and destination encoders-lossless and lossy compression-entropy encoding –source encoding -text compression –static Huffman coding dynamic coding –arithmetic coding –Lempel ziv-welsh Compression-image compression.		
UNIT IV	**VOIP TECHNOLOGY**	**9**
Basics of IP transport, VoIP challenges, H.323/ SIP –Network Architecture, Protocols,Call establishment and release, VoIP and SS7, Quality of Service- CODEC Methods- VOIP		

applicability.		
UNIT V	**MULTIMEDIA NETWORKING**	**9**
Multimedia networking -Applications-streamed stored and audio-making the best Effort service-protocols for real time interactive Applications-distributing multimedia-beyond best effort service-secluding and policing Mechanisms-integrated services-differentiated Services-RSVP.		
	TOTAL : 45 PERIODS	

OUTCOMES	Upon completion the course , the students will have the ability to
1.	Describe various multimedia components.
2.	Analyze audio and video compression techniques.
3.	Describe the text and image compression techniques.
4.	Analyse the VOIP technology.
5.	Design multimedia networking.

TEXTBOOKS	
1.	R. Steimnetz, K. Nahrstedt, "Multimedia Computing, Communications and Applications", Pearson Education Ranjan Parekh, "Principles of Multimedia", TMH 2007.
2.	Fred Halshall "Multimedia communication - Applications, Networks, Protocols and Standards", Pearson Education, 2007.
3.	Tay Vaughan, "Multimedia: Making it work", 7th Edition, TMH 2008 98

REFERENCES	
1.	*Wolfegang Effelsberg, "Video Compression Techniques", Elsevier.*
2.	*Marcus Goncalves "Voice over IP Networks", Mc Graw hill 1999.*
3.	*KR. Rao,Z S Bojkovic, D A Milovanovic, "Multimedia Communication Systems: Techniques, Standards, and Networks", Pearson Education 2007.*
4.	*Kurose and W.Ross "Computer Networking "a Top Down Approach", Pearson Education 2005*

AUDIT COURSES

18ZAC001	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humani multiple perspectives tarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

UNIT I	INTRODUCTION	5

Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

UNIT II	REPERCUSSIONS OF DISASTERS AND HAZARDS	5

Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III	DISASTER PRONE AREAS IN INDIA	5

Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

UNIT IV	DISASTER PREPAREDNESS AND MANAGEMENT	5

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

UNIT V	RISK ASSESSMENT	5

Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

UNIT VI	DISASTER MITIGATION	5

Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	
	TOTAL : 30 PERIODS
OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Application of Disaster Concepts to Management.
2.	Analyze Relationship between Development and Disasters.
3.	Ability to Categories Disasters and Preparedness plans for disaster response.
4.	Monitoring and evaluation plan for disaster response and Setting up of early warning systems for risk reductions
5.	Acquainting with Disaster Response command system in respective states and Application of Best Practices from Case scenario Studies in India
REFERENCES:	
1.	*R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.*
2.	*Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.*
3.	*Goel S. L., Disaster Administration And Management Text And Case Studies",Deep &Deep Publication Pvt. Ltd., New Delhi.*

18ZAC002	**ENGLISH FOR RESEARCH PAPER WRITING**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title

UNIT I		**5**
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness		

UNIT II		**5**
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction		
UNIT III		**5**
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.		
UNIT IV		**5**
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,		
UNIT V		**5**
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions		
UNIT VI		**5**
useful phrases, how to ensure paper is as good as it could possibly be the first- time submission		
		TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Write technical papers on their own.
2.	Planning preparation of content for papers.
3.	Knowledge of what to be highlighted.
4.	Review of a literatures
5.	Key skills needed for writing papers.

REFERENCES:	
1.	*Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)*
2.	*Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM.*
3.	*Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011*

18ZAC003	RESEARCH METHODOLOGY AND IPR	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Definition and objectives of Research
- Quantitative methods for problem solving
- Data description and report writing

UNIT I	RESEARCH METHODOLOGY AND DATA COLLECTION	6

Research methodology - definition, mathematical tools for analysis. Types of research exploratory research, conclusive research, modelling research, algorithmic research, Research process - steps. Data collection methods - primary data - observation method personal interview, telephonic interview, mail survey, questionnaire design. Secondary data - internal sources of data, external sources of data.

UNIT II	SCALES AND SAMPLING	6

Scales - Measurement, Types of scale - Turnstone's Case V scale model, Osgood's Semantic Differential scale, Likert scale. Q-sort scale. Sampling methods - Probability sampling methods – simple random sampling with replacement, simple random sampling without replacement, Stratified sampling, cluster sampling. Non-probability sampling method - convenience sampling, judgment sampling quota sampling.

UNIT III	HYPOTHESES	6

Hypotheses testing- Testing of hypotheses concerning means (one mean and difference between two means- one tailed and two tailed tests) , Concerning variance one tailed Chi-square test.

UNIT IV	NONPARAMETRIC TESTS	6

Nonparametric tests- One sample tests - one sample tests- on sample sign test, Kolmogorov-Smirnov test, run test for randomness, Two sample test - Two sample sign test, Mann- Whitney U test, K-sample test - Kruskal Wallis test (H-Test)

UNIT V	DISCRIMINANT ANALYSIS	6

Introduction to Discriminant analysis, Factor analysis, cluster analysis, multi-dimensional scaling, conjoint analysis. Report writing- Types of report, guidelines to review report, typing instructions, oral presentation.

TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:

1.	Aware of basic research process, research methodology.
2.	Apply Knowledge of hypotheses, Non-parametric Tests
3.	Develop research question
4.	Perform exhaustive literature survey
5.	Apply right problem solving methods

REFERENCES:

1.	*Kothari. C.R., "Research Methodology - Methods and techniques", New Age Publications, New Delhi, 2009*
2.	*Panneerselvam, R., "Research Methodology", Prentice-Hall of India. New Delhi, 2004.*

18ZAC004	**SANSKRIT FOR TECHNICAL KNOWLEDGE**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects

UNIT I		**10**
Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences		
UNIT II		**10**
Order, Introduction of roots, Technical information about Sanskrit Literature		
UNIT III		**10**
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics		

	TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Understanding basic Sanskrit language
2.	Ancient Sanskrit literature about science & technology can be understood
3.	Being a logical language will help to develop logic in students

REFERENCES:	
1.	*"Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi*
2.	*"Teach Yourself Sanskrit" Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication*
3.	*"India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.*

18ZAC005	**VALUE EDUCATION**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

UNIT I		**6**
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgments		

UNIT II		**8**
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline		

UNIT III		8
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature		
UNIT IV		8
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively		
		TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Knowledge of self-development
2.	Learn the importance of Human values
3.	Developing the overall personality
REFERENCES:	
1.	*Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi*

18ZAC006	**PEDAGOGY STUDIES**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

UNIT I		**6**
INTRODUCTION AND METHODOLOGY: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching		
UNIT II		**6**
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.		
UNIT III		**6**
Evidence on the effectiveness of pedagogical practices Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.		
UNIT IV		**6**
Professional development: alignment with classroom practices and follow-up support Peer support Support from the head teacher and the community. Curriculum and assessment Barriers to learning: limited resources and large class sizes		
UNIT V		**6**
RESEARCH GAPS AND FUTURE DIRECTIONS : Research design Contexts Pedagogy Teacher education Curriculum and assessment Dissemination and research impact.		
		TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2.	What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3.	How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

REFERENCES:	
1.	*Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.*
2.	*Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.*

3.	*Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston:Blackwell*
4.	*Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign*

18ZAC007	**STRESS MANAGEMENT BY YOGA**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- To achieve overall health of body and mind
- To overcome stress.

UNIT I		**10**
Definitions of Eight parts of yog. (Ashtanga)		
UNIT II		**10**
Yam and Niyam. Do`s and Don't's in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan		
UNIT III		**10**
Asan and Pranayam i) Various yog poses and their benefits for mind & body ii)Regularization of breathing techniques and its effects-Types of pranayam		
		TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Develop healthy mind in a healthy body thus improving social health also
2.	Improve efficiency

REFERENCES:	
1.	*Yogic Asanas for Group Tarining-Part-I" :Janardan Swami Yogabhyasi Mandal, Nagpur*
2.	*Rajayoga or conquering the interrnal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata*

18ZAC008	**PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- To learn to achieve the highest goal happily.
- To become a person with stable mind, pleasing personality and determination.
- To awaken wisdom in students.

UNIT I		**10**

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT II		**10**

Approach to day to day work and duties. Shrimad BhagwadGeeta :

- Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35,
- Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT III		10
Statements of basic knowledge. Shrimad BhagwadGeeta: • Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 Personality of Role model. Shrimad BhagwadGeeta: • Chapter2-Verses 17, • Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63		
		TOTAL : 30 PERIODS

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2.	The person who studied Geeta will lead the nation and mankind to peace and prosperity
3.	Study of Neetishatakam will help in developing versatile personality of students.

REFERENCES:	
1.	*"Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata*
2.	*Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.*

18ZAC009	ELECTRONIC WASTE MANAGEMENT	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- To understand the techniques used in E-waste management.

UNIT I		10
E-waste Overview, E-waste Management Overview		
UNIT II		**10**
Environmental and Public health issues, E-waste health risk assessment		
UNIT III		**10**
Recovery of material form E-waste, Material Recovery Process, electronics and LCA, LCA applications for electronics		
	TOTAL : 30 PERIODS	

OUTCOMES:	Upon completion of this course, the students will be able to:
1.	Define E-waste management techniques.
2.	Define the process of material recovery

REFERENCES:	
1.	*Electronic Waste Management Rules 2016, Govt. of India, available online at CPCB website.*
2.	*MSW Management Rules 2016, Govt. of India, available online at CPCB website.*
3.	*Scientific literature uploaded by TAs*