GOVERNMENT COLLEGE OF ENGINEERING, BARGUR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(ACCREDITED BY NBA)

P.G. FULLTIME

M.E. - APPLIED ELECTRONICS

CURRICULUM & SYLLABI

(REGULATIONS – 2017)

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR

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GOVERNMENT COLLEGE OF ENGINEERING, BARGUR

DEPARTMENT OF ECE

VISION OF THE INSTITUTE

To provide world class engineers who are ethical and good citizens of our motherland

MISSION OF THE INSTITUTE

To groom the student community through learner centric quality lectures, laboratories, Library and value added training.

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR

DEPARTMENT OF ECE

VISION OF THE DEPARTMENT

We envision our students to be excellent engineers not only in the field of science and technology, but also embed the greatest values of human life. Our commitment lies in producing good citizens, comprehensive knowledge seekers and remains as an asset in building a strong and developed nation.

MISSION OF THE DEPARTMENT

- To achieve the vision we should have hard working faculty who use effective teaching methodologies.
- To impart knowledge in the latest trends of technical education.
- To prepare our young students to become professionally and morally sound engineers.
- To teach global standards in production and value based living through a truthful and technical approach.

PROGRAM EDUCATIONAL OBJECTIVES (PEO)

PEO1. To demonstrate the education skills that will enable to integrate fundamentals with advanced knowledge to provide solutions to complex electronics engineering problems.

PEO2. To provide a successful career in electronic system design or associated industries or research and higher education, or as entrepreneurs.

PEO3. To develop the ability and attitude to adapt to evolving technological challenges

PROGRAMME OUTCOMES (PO)

a) Graduates will demonstrate knowledge of fuzzy logic and matrix theory, random variables and probability functions, dynamic programming and queuing models.

b) Graduates will demonstrate an ability to identify, analyze and develop solutions to solve complex problems using digital signal processing techniques.

c) Graduates will demonstrate an ability to design advanced digital circuits and analyze them through Simulation and practice.

d) Graduates will demonstrate an ability to design digital and analog VLSI circuits and analyze them through simulation and practice and to understand and program advanced microprocessors and microcontrollers and analyze them for embedded applications.

e) Graduates will demonstrate an ability to visualize and work on laboratory and multi-disciplinary tasks.

f) Graduates will demonstrate skills to use modern electronics design and simulation tools (both software and hardware) to analyze problems.

g) Graduates will demonstrate knowledge of professional and ethical responsibilities.

h) Graduates will be able to communicate effectively in both verbal and written form.

i) Graduates will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues.

j) Graduates will develop confidence for self-education and ability for lifelong learning.

k) Graduates will be able to participate and succeed in competitive examinations.

l) Graduates will demonstrate an ability as an individual or as a member of a team to solve complex and socially relevant engineering problems.

GOVERNMENT COLLEGE OF ENGINEERING
BARGUR

Regulation – 2017

AUTONOMOUS

Curriculum for Full Time M.E.–Applied Electronics
(Department of ECE)
From the Academic Year 2017 -2018 onwards

SEMESTER-I

SL.No.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1.	17AEFC01	Applied Mathematics for Electronics Engineers	FC	4	0	0	4
2.	17AEPC02	Advanced Digital System Design	PC	3	0	0	3
3.	17AEPC03	Advanced Digital Signal Processing	PC	3	2	0	4
4.	17AEPC04	Embedded System Design	PC	3	0	0	3
5.	17AEPC05	Modern communication techniques	PC	3	0	0	3
6.		Professional Elective I	PC	3	0	0	3
PRACTICALS							
7.	17AEPC06	Embedded System Design Laboratory	PC	0	0	4	2
			TOTAL	**12**	**2**	**4**	**22**

SEMESTER-II

SL.No.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1.	17AEPC07	Soft Computing and Optimization Techniques	PC	3	0	0	3
2.	17AEPC08	VLSI System Design	PC	3	0	0	3
3.	17AEPC09	Hardware – Software Co-design	PC	3	0	0	3
4.	17AEPC10	Internet of Things	PC	3	0	0	3
5.		Professional Elective II	PE	3	0	0	3
6.		Professional Elective III	PE	3	0	0	3
PRACTICALS							
7.	17AEPC11	VLSI System Design Laboratory	PC	0	0	4	2
8.	17AEEE12	Term Paper Writing and Seminar	EEC	0	0	2	1
			TOTAL	**18**	**0**	**6**	**21**

SEMESTER-III

SL.No.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1.	17AEPC13	Electronic Product design and development	PC	3	0	0	3
2.		Professional Elective IV	PE	3	0	0	3
3.		Professional Elective V	PE	3	0	0	3
PRACTICALS							
4.	17AEEE14	Project Work Phase I	EEC	0	0	12	6
			TOTAL	**12**	**0**	**12**	**15**

SEMESTER-IV

SL.No.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
PRACTICALS							
1.	17AEEE15	Project Work Phase II	EEC	0	0	24	12
			TOTAL	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 70

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

SL.NO	COURSE CODE	COURSETITLE	L	T	P	C
1.	17AEEE12	Term Paper Writing and Seminar	0	0	2	1
2.	17AEEE14	Project Work Phase I	**0**	**0**	**12**	**6**
3.	17AEEE15	Project Work Phase II	**0**	**0**	**24**	**12**

PROFESSIONAL ELECTIVES (PE)

SEMESTER I

ELECTIVE I

SL.NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	17AEPE01	Digital Control Engineering	PE	**3**	**0**	**0**	**3**
2.	17AEPE02	Computer Architecture	PE	**3**	**0**	**0**	**3**
3.	17AEPE03	Digital VLSI design	PE	**3**	**0**	**0**	**3**
4.	17AEPE04	Electromagnetic Interference and Compatibility	PE	**3**	**0**	**0**	**3**

PROFESSIONAL ELECTIVES (PE)

SEMESTER II

ELECTIVE II

SL.NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	17AEPE05	CAD for VLSI	PE	**3**	**0**	**0**	**3**
2.	17AEPE06	Nano Electronics	PE	**3**	**0**	**0**	**3**
3.	17AEPE07	Sensors and measurement systems	PE	**3**	**0**	**0**	**3**
4.	17AEPE08	MEMS and NEMS	PE	**3**	**0**	**0**	**3**

SEMESTER II

ELECTIVE III

SL.NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	17AEPE09	DSP processor Architectures and Programming	PE	**3**	**0**	**0**	**3**
2.	17AEPE10	RF System Design	PE	**3**	**0**	**0**	**3**
3.	17AEPE11	Speech Signal Processing	PE	**3**	**0**	**0**	**3**
4.	17AEPE12	Solid State Device Modeling and simulation	PE	**3**	**0**	**0**	**3**

SEMESTER III

ELECTIVE IV

SL.NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	17AEPE13	Advanced Microprocessor and Microcontroller Architecture	PE	**3**	**0**	**0**	**3**
2.	17AEPE14	System on Chip Design	PE	**3**	**0**	**0**	**3**
3.	17AEPE15	Robotics	PE	**3**	**0**	**0**	**3**
4.	17AEPE16	Physical Design of VLSI Circuits	PE	**3**	**0**	**0**	**3**
5.	17AEPE17	High Performance Networks	PE	**3**	**0**	**0**	**3**

SEMESTER III

ELECTIVE V

SL.NO	COURSE CODE	COURSETITLE	CATEGORY	L	T	P	C
1.	17AEPE18	Pattern Recognition	PE	**3**	**0**	**0**	**3**
2.	17AEPE19	Secure Computing Systems	PE	**3**	**0**	**0**	**3**
3.	17AEPE20	Signal Integrity for High Speed Design	PE	**3**	**0**	**0**	**3**
4.	17AEPE21	Wireless AD-HOC and Sensor Networks	PE	**3**	**0**	**0**	**3**

SEMESTER- I

17AEFC01	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C
		4	0	0	4

OBJECTIVES:

- To impart knowledge on fuzzy logic.
- To understand the basic concepts of matrix theory and their applications.
- To find the optimum solution of the random variables.
- To understand the concepts of dynamic programming and queuing models.

UNIT I	FUZZY LOGIC	9

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II	MATRIX THEORY	9

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization – Least squares method - Singular value decomposition.

UNIT III	PROBABILITY AND RANDOM VARIABLE	9

Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables -Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.

UNIT IV	DYNAMIC PROGRAMMING	9

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V	QUEUEING MODELS	9

Poisson Process – Markovian queues – Single and multi server models – Little's formula – Machine interference model – Steady state analysis – Self service queue.

TOTAL:60 PERIODS

OUTCOMES:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.

•	Apply various methods in matrix theory to solve system of linear equations.
•	Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
•	Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
•	Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models
•	Using discrete time Markov chains to model computer systems.

REFERENCES:

1.	*Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.*
2.	*George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.*
3.	*Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.*
4.	*Johnson, R.A., Miller, I and Freund J., Miller and Freunds "Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.*
5.	*Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia, NewDelhi, 2016.*

17AEPC02	**ADVANCED DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**C**

	3	**0**	**0**	**3**

OBJECTIVES:

- To analyze synchronous and asynchronous sequential circuits
- To realize and design hazard free circuits
- To familiarize the practical issues of sequential circuit design
- To gain knowledge about different fault diagnosis and testing methods
- To estimate the performance of digital systems
- To know about timing analysis of memory and PLD

UNIT I	**SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM

UNIT II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of synchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**	**9**

Fault table method-path sensitization method – Boolean difference method-D algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**	**9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 400

UNIT V	**SYSTEM DESIGN USING VERILOG**	**9**

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench -Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

	TOTAL : 45 PERIODS

OUTCOMES:

•	Analyze and design sequential digital circuits
•	Identify the requirements and specifications of the system required for a given application
•	Identify the fault diagnosis.
•	Realize and design hazard free circuits.
•	Design the logic system using VHDL

REFERENCES:

1.	*C. H.Roth Jr and L.L.Kinney,"Fundamentals of Logic Design" Cengage Learning ,2004*
2.	*M.D.Ciletti , "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice Hall, 1999.*
3.	*M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.*
4.	*N. N. Biswas "Logic Design Theory" Prentice Hall of India,2001*
5.	*P. K.Lala "Digital system Design using PLD" B S Publications,2003*
6.	*P.K..Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002*
7.	*S. Palnitkar , "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson , 2003.*

17AEPC03	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	2	0	4

OBJECTIVES:

•	To get in-depth knowledge about Discrete-time signal transforms.
•	To analyse the Power spectrum estimation.
•	To learn DSP architectures which are of importance in the areas of signal processing, control and communications
•	To understand digital filter design and optimal filtering technique.
•	To analyse different multi-rate digital signal processing technique.

UNIT I	DISCRETE RANDOM SIGNAL PROCESSING	12

Wide sense stationary process – Ergodic process – Mean – Variance - Auto-correlation and Auto-covariance matrix - Properties - Weiner Khintchine relation - Power spectral density – filtering random process, Spectral Factorization Theorem–Finite Data records, Simulation of uniformly distributed/Gaussian distributed white noise – Simulation of Sine wave mixed with Additive White Gaussian Noise.

UNIT II	SPECTRUM ESTIMATION	12

Bias and Consistency of estimators - Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysis of estimators – Unbiased consistent estimators - Periodogram estimator - Barlett spectrum estimation - Welch estimation.

UNIT III	LINEAR ESTIMATION AND PREDICTION	12

Model based approach - AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker method - Maximum likelihood criterion - Efficiency of estimator - Least mean squared error criterion – Wiener filter - Discrete Wiener Hoff equations – Mean square error.

UNIT IV	ADAPTIVE FILTERS	12

Recursive estimators - Kalman filter - Linear prediction – Forward prediction and Backward prediction, Prediction error - Whitening filter, Inverse filter - Levinson recursion, Lattice realization, Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT V	MULTIRATE DIGITAL SIGNAL PROCESSING	12

FIR Adaptive filters - Newton's steepest descent method - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS –

Sliding window RLS - Simplified IIR LMS Adaptive filter.	
	TOTAL45+15: 60 PERIODS
OUTCOMES:	
•	Exposed to different discrete signal processing methods.
•	Understanding different spectral estimation techniques.
•	Apply linear estimation techniques and linear prediction.
•	To design adaptive filters for a given application.
•	To design multirate DSP systems.
REFERENCES:	
1.	*J. G. Proakis, D.G. Manolakis, "Digital Signal Processing", Prentice Hall of India, New Delhi, 2005.*
2.	*M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons In, New York, 2006.*
3.	*P. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1992.*
4.	*S. Kay," Modern spectrum Estimation theory and application", Prentice Hall, Englehood Cliffs, NJ1988.*
5.	*S. Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986.*
6.	*S. J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.*

17AEPC04	EMBEDDED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the design challenges about embedded system.
- To learn various techniques of system processor.
- To outline various protocols.
- To understand different state machine and process models.
- To afford awareness about Hardware and software design architecture for embedded processors with real time examples.

UNIT I	EMBEDDED SYSTEM OVERVIEW	9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II	GENERAL AND SINGLE PURPOSE PROCESSOR	9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III	BUS STRUCTURES	9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV	STATE MACHINE AND CONCURRENT PROCESS MODELS	9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS..

	TOTAL : 45 PERIODS
OUTCOMES:	
•	Discuss design challenges and various architecture of embedded system.
•	Analyse the different Embedded Processors
•	Analyse the real time characteristics of embedded processors.
•	Discuss state machine and design process models
•	Outline embedded software development tools and RTOS
REFERENCES:	
1.	*B.P. Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.*
2.	*D.W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.*
3.	*F. Vahid and T.Gwargie, "Embedded System Design", John Wiley & sons, 2002.*
4.	*S. Heath, "Embedded System Design", Elsevier, Second Edition, 2004.*

7AEPC05	MODERN COMMUNICATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To estimate the power spectra of different modulation techniques.
- To learn coherent and non-coherent communication.
- To analyze digital modulation techniques over band limited channels.
- To apply various channel coding techniques.
- To apply various decoding algorithm.

UNIT I	POWER SPECTRUM AND COMMUNICATION OVER MEMORYLESS CHANNEL	9

PSD of a Synchronous Data Pulse Stream – M–ary Markov source – Convolutionaly Coded Modulation – Continuous Phase Modulation – Scalar and Vector Communication over Memory less Channel – Detection Criteria.

UNIT II	COHERENT AND NON –COHERENT COMMUNICATION	9

Coherent Receivers – Optimum Receivers in WGN – IQ Modulation & Demodulation – Non–Coherent receivers in Random Phase Channels – M–FSK Receivers – Rayleigh and Rician Channels – Partially Coherent Receivers – DPSK – M –PSK – M –DPSK – BER Performance Analysis.

UNIT III	BANDLIMITED CHANNELS AND DIGITAL MODULATIONS	9

Eye pattern – Demodulation in the presence of ISI and AWGN – Equalization techniques – IQ modulations – QPSK – QAM – QBOM – BER Performance Analysis – Continuous Phase Modulation – CPFM – CPFSK – MSK – OFDM

UNIT IV	BLOCK CODED DIGITAL COMMUNICATION	9

Architecture and Performance – Binary Block Codes – Orthogonal – Bi–orthogonal – Trans–orthogonal – Shannon's Channel Coding Theorem – Channel Capacity – Matched Filter – Concepts of Spread Spectrum Communication – Coded BPSK and DPSK Demodulators – Linear Block Codes – Hamming–Golay Cyclic – BCH – Reed– Solomon Codes

UNIT V	CONVOLUTIONAL CODED DIGITAL COMMUNICATION	9

Representation of Codes using Polynomial – State Diagram – Tree Diagram and Trellis Diagram – Decoding Techniques using Maximum Likelihood – Viterbi Algorithm – Sequential and Threshold

methods – Error probability performance for BPSK and Viterbi Algorithm – Turbo Coding	
	TOTAL : 45 PERIODS

OUTCOMES:

•	Discuss various power spectra of communication channels.
•	Discuss coherent and non-coherent communication.
•	Discuss various digital modulation schemes.
•	Discuss various coding techniques.
•	Design different coding methods.

REFERENCES:

1.	*Simon M. K., Hinedi S. M. and Lindsey W. C., "Digital Communication Techniques, Signaling and Detection", Prentice Hall India, 1995.*
2.	*S. Haykin, "Digital communications", John Wiley and Sons, 1998.*
3.	*W. Tomasi, "Advanced Electronic Communication Systems", 4th Edition, Pearson Education , 1998.*
4.	*Lathi B. P., "Modern Digital and Analog Communication Systems", 3rd Edition, Oxford University Press, 1998.*

17AEPC06	EMBEDDED SYSTEM DESIGN LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

•	To analyze Synchronous and Asynchronous sequential circuits.
•	To design system using 8086 and 8051 Microcontroller.
•	To study different interfaces using embedded Microcontroller.
•	To design and analysis of real time signal processing system.
•	To implement various equalization and coding technique.

LIST OF EXPERIMENTS:

1.	System design using PIC, MSP430, 51 Microcontroller and 16- bit Microprocessor - 8086.
2.	Study of different interfaces (using embedded microcontroller).
3.	Implementation of Adaptive Filters and multistage multirate system in DSP Processor.
4.	Simulation of QMF using Simulation Packages.
5.	Study of 32 bit ARM7 microcontroller RTOS and its application
6.	Testing RTOS environment and system programming
7.	Designing of wireless sensor network using embedded systems
8.	Design and analysis of real time signal processing system – Data acquisition and signal processing
9.	Implementation of Equalization and coding techniques using software defined radio.
	TOTAL : 60 PERIODS

OUTCOMES:

•	Apply PIC, MSP430, "51 Microcontroller and 8086 for system design.
•	Simulate QMF.
•	Utilize ARM with FPGA
•	Design and analyze of real time signal processing system.
•	Implement various coding technique.

SEMESTER -II

17AEPC07	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	L	T	P	C
		4	0	0	4

OBJECTIVES:

•	To learn various Soft computing frameworks.
•	To familiarizes with the design of various neural networks.
•	To understand the concept of fuzzy logic.
•	To gain insight onto Neuro Fuzzy modelling and control.
•	To gain knowledge in conventional optimization techniques.
•	To understand the various evolutionary optimization techniques

UNIT I	NEURAL NETWORKS	9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network

UNIT II	FUZZY LOGIC	9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

UNIT III	NEURO-FUZZY MODELING	9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

UNIT IV	CONVENTIONAL OPTIMIZATION TECHNIQUES	9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V	EVOLUTIONARY OPTIMIZATION TECHNIQUES	9
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	Implement machine learning through Neural networks.
•	Develop a Fuzzy expert system.
•	Understand the various evolutionary optimization techniques
•	Model Neuro Fuzzy system for clustering and classification.
•	Able to use the optimization techniques to solve the real world problems

REFERENCES:

1.	*D. E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison wesley,1989.*
2.	*G. J. Klir and B.Yuan, "Fuzzy Sets and Fuzzy Logic-Theory and Applications",Prentice Hall, 1995.*
3.	*J.A. Freeman and D. M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Edn., 2003.*
4.	*J. R. Jang, C.T. Sun, E. Mizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.*
5.	*M. Melanie, "An Introduction to Genetic Algorithm", Prentice Hall, 1998.*
6.	*S. Haykins, "Neural Networks: A Comprehensive Foundation", Prentice Hall International Inc, 1999.*
7.	*S. S. Rao, "Engineering optimization Theory and practice", John Wiley & sons, inc,Fourth Edition, 2009*
8.	*T. J.Ross, "Fuzzy Logic with Engineering Applications", McGraw-Hill, 1997.*
9.	*V. Rao, V. J. Savsani, "Mechanical Design Optimization Using Advanced Optimization Techniques", Springer ,2012.*

17AEPC08	VLSI SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC
- To analyse the synthesis, Simulation and testing of systems.
- To understand the design issues of SOC.
- To know about different high performance algorithms and its applications in ASICs.

UNIT I	OVERVIEW OF ASIC AND PLD	9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II	ASIC PHYSICAL DESIGN	9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC.

UNIT III	LOGIC SYNTHESIS, SIMULATION AND TESTING	9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV	FIELD PROGRAMMABLE GATE ARRAYS	9

FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT V	SOC DESIGN	9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

	TOTAL : 45 PERIODS

OUTCOMES:

•	Apply different high performance algorithms in ASICs.
•	Be familiar the different types of programming technologies and logic devices.
•	Analyze the synthesis, Simulation and testing of systems.
•	Have the knowledge of FPGA.
•	Discuss the design issues of SOC.

REFERENCES:

1.	*D.A.Hodges, " Analysis and Design of Digital Integrated Circuits (3/e)|, MGH, 2004.*
2.	*H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999 .*
3.	*J. M. Rabaey , " Digital Integrated Circuit Design Perspective (2/e)", PHI, 2003*
4.	*M.J.S. Smith , "Application Specific Integrated Circuits", Pearson, 2003*
5.	*J. O.Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley& Sons, Newyork,1995.*
6.	*P.K.Chan& S. Mourad, "Digital Design using Field Programmable Gate Array", Prentice Hal,1994.*
7.	*S. Pasricha and NikilDutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008*
8.	*S.Trimberger , " Field Programmable Gate Array Technology", Kluwer Academic Pub,1994.*
9.	*S.Brown,R.Francis, J.Rose, Z.Vransic, "Field Programmable GateArray", BS,2007.*

17AEPC09	HARDWARE - SOFTWARE CO-DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To acquire the knowledge about system specification and modelling.
- To estimate the hardware/software partitioning.
- To study the different technical aspects about prototyping and emulation.
- To learn the hardware/software co-synthesis.
- To verify and design various system level specification languages.

UNIT I	SYSTEM SPECIFICATION AND MODELLING	9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II	HARDWARE / SOFTWARE PARTITIONING	9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III	HARDWARE / SOFTWARE CO-SYNTHESIS	9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT IV	PROTOTYPING AND EMULATION	9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V	DESIGN SPECIFICATION AND VERIFICATION	9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

	TOTAL : 45 PERIODS

OUTCOMES:	
•	Design of system specification and modelling.
•	Assess prototyping and emulation techniques.
•	Outline various hardware and software partitioning problem.
•	Compare hardware / software co-synthesis.
•	Formulate the design specification and validate its functionality by simulation.
REFERENCES:	
1.	*G. D.Micheli , R. E. Morgon, "Reading in Hardware/Software Co-Design" Kaufmann Publishers,2001.*
2.	*J. Staunstrup, W. Wolf , "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.*
3.	*R. Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.*

17AEPC10	INTERNET OF THINGS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using Raspberry Pi.
- To learn about the basics of IOT architecture.
- To apply the concept of Internet of Things in the real world scenario

UNIT I	INTRODUCTION TO IoT	9

Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

UNIT II	IoT ARCHITECTURE	9

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture

UNIT III	IoT PROTOCOLS	9

Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – 6LowPAN - CoAP - Security

UNIT IV	BUILDING IoT WITH RASPBERRY PI&ARDUINO	9

Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino.

UNIT V	SIMULATION OF DEVICES	9

Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.

	TOTAL : 45 PERIODS
OUTCOMES:	
•	Analyze various protocols for IoT
•	Develop web services to access/control IoT devices.
•	Design a portable IoT using Rasperry Pi
•	Deploy an IoT application and connect to the cloud.
•	Analyze applications of IoT in real time scenario
REFERENCES:	
1.	*A. Bahga, V. Madisetti, "Internet of Things – A hands-on approach", Universities Press, 2015*
2.	*D. Uckelmann, M. Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011.*
3.	*H. Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.*
4.	*J. Holler, V. Tsiatsis , C. Mulligan, Stamatis , Karnouskos, S. Avesand, D. Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.*
5.	*O. Hersent, D. Boswarthick, O. Elloumi , "The Internet of Things – Key applications and Protocols", Wiley, 2012*

17AEPC11	VLSI SYSTEM DESIGN LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

•	To analyze synchronous and asynchronous sequential circuits.
•	To design and implement ALU in FPGA using VHDL.
•	To design ,simulate and analyze the signal integrity.
•	To assess flash controller programming - data flash with erase, verify and fusing
•	To design sensor using simulation tools

LIST OF EXPERIMENTS:

1.	Analysis of Asynchronous and clocked synchronous sequential circuits.
2.	Testing and Fault diagnosis of VLSI circuits.
3.	VHDL/VERILOG implementation of temperature sensor.
4.	Design, Simulation and analysis of Signal Integrity.
5.	VHDL/VERILOG implementation of I2C , SPI Interfacing.
6.	Design and Implementation of ALU in FPGA using VHDL and Verilog.
7.	Modeling of Sequential Digital system using Verilog and VHDL.
8.	Flash controller programming - data flash with erase, verify and fusing.
	TOTAL : 60 PERIODS

OUTCOMES:

•	Design sensor using simulation tools.
•	Explain design, simulation and analysis of signal integrity
•	Demonstrate design of ALU in FPGA using VHDL and Verilog
•	Assess flash controller programming - data flash with erase, verify and fusing
•	Analyse synchronous and asynchronous sequential circuits.

SEMESTER -III

17AEPC13	ELECTRONIC PRODUCT DESIGN AND DEVELOPMENT	L	T	P	C
		3	0	0	3

OBJECTIVES:

•	To learn the electronic product design and development stages.
•	To apply fundamentals of PCB and PCB design.
•	To test and debug hardware/software design.
•	To test different electronic products.
•	To learn different types of standards.

UNIT I	PRODUCT DESIGN AND DEVELOPMENT	9

Introduction, Product development basics, Product development stages, Identification of the customer requirements, Designing the product ,Techno-commercial feasibility of a product, Pilot production batch, Product assessment, Availability, Screening test of component, redundancy, Effects of environmental conditions on reliability, Comparison between repairable and non-repairable systems, Failure rates of electronic components, Ergonomic and aesthetic design considerations.

UNIT II	FUNDAMENTALS OF PCB	9

Introduction to PCBs, Layout, Issues related to PCB size, Interconnection parameters, Recommendations for Power and ground traces routing, PCB design for digital circuits, Noise due to ground and supply line, Grounds, Returns and Shields, PCB design rules for analog circuits, Design issues related to supply and ground conductors, Multilayer Boards, Component assembly techniques, Testing of assembled PCBs, Board layout checklist, Bare board testing, Testing of multilayer PCB, Compare of PCBs.

UNIT III	PCB DESIGN	9

Introduction, Computer-aided design, Automation in design, Soldering techniques, Soldering testing, Packages for semiconductor devices and ICs, Reliability issues in ICs, Parastic elements, High-speed PCBs and parasitic elements, PCB designing for microprocessor-based circuits, High speed PCB design, Design consideration in high speed PCBs, Component mounting under vibration ,SMDs, Cable.

UNIT IV	HARDWARE, SOFTWARE DESIGN AND TESTING METHODS	9

Introduction, Logic analyzer, uses of logic analyze, Oscilloscope Probes, Signal integrity, Use and limitation of Different types of analysis, SPICE, Monte-Carlo analysis, evolution of virtual

instrumentation. Introduction, Phases of software design, Goals of software design, Design of Structured program, Testing and debugging of program, Algorithmic state machine, Finite state machines, Selection of language for software development, Assemblers, Compilers, Simulators, Emulators.		
UNIT V	**ELECTRONIC PRODUCT TESTING**	**9**
Introduction, Environmental testing, Temperature testing, Thermal modelling of components, Humidity testing, Electrical overstress testing, Altitude testing, Special testing, Environmental test chambers and rooms, Various test on enclosures, EMI and EMC related testing, EMC and Compliance, Conducted emission test using time domain principle, Radiated emission test, Importance of standards, Standards and Standard developing organisations, List of some standards, CE marking and certification, UL marking and certification, IEC standards, IEC safety standards: CAT standards.		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	Design electronic products
•	Apply fundamentals of PCB and PCB design
•	Implement and Test hardware design
•	Model Software design and testing
•	Prepare product documentation

REFERENCES:

1.	*R.G.Kaduskar,V.B.Baru, "Electronic Product design", 2nd Edition,Wiley,2011.*
2.	*B.Haskell, "Portable Electronics Product design and development", Mcgraw hill publisher,2004.*
3.	*P.Horowitz, "The Art of Electronics",Harvard university,2015.*
4.	*https://www.amazon.com/Electronic-Product-Design-V-B-Kaduskar-ebook/dp/B01LZF18QV*

17AEEE14	PROJECT WORK PHASE I	L	T	P	C
		0	0	12	6

OBJECTIVES:

•	To develop the ability to solve a specific problem right from its identification and literature review till the successful solution of the same.
•	To train the students in preparing project reports and to face reviews and viva voce examination.

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

GUIDELINES FOR DISSERTATION PHASE – I

- As per the AICTE directives, the dissertation is a year long activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December.
- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics

and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred
and reported.

- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

	TOTAL : 180 PERIODS

OUTCOMES:

•	Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem
•	Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
•	Ability to present the findings of their technical solution in a written report.

SEMESTER- IV

17AEEE15	PROJECT WORK PHASE II	L	T	P	C
		0	0	24	12

OBJECTIVES:

•	To develop the ability to solve a specific problem right from its identification and literature review till the successful solution of the same.
•	To train the students in preparing project reports and to face reviews and viva voce examination.

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

GUIDELINES FOR DISSERTATION PHASE – II

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June .

- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals or reviewed focused conferences or IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.

	TOTAL : 360 PERIODS

OUTCOMES:	
•	Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem
•	Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
•	Ability to present the findings of their technical solution in a written report.
•	Presenting the work in International/ National conference or reputed journals.

PROFESSIONAL ELECTIVES (PE)

SEMESTER- I

ELECTIVE I

17AEPE01	DIGITAL CONTROL ENGINEERING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the principles of PI,PD,PID controllers
- To analyse time and frequency response of discrete time control system
- To be familiar in digital control algorithms.
- To get basic knowledge to implement PID control algorithms.
- To learn the basic DSP in control system.

UNIT I	CONTROLLERS IN FEEDBACK SYSTEMS	9

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

UNIT II	BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS	9

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction

UNIT III	MODELING OF SAMPLED DATA CONTROL SYSTEM	9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV	DESIGN OF DIGITAL CONTROL ALGORITHMS	9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V	PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS	9
Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	Describe continuous time and discrete time controllers analytically.
•	Define and state basic analog to digital and digital to analog conversion principles.
•	Analyze sampled data control system in time and frequency domains.
•	Design simple PI, PD, PID continuous and digital controllers.
•	Develop schemes for practical implementation of temperature and motor control systems.

REFERENCES:

1.	*J. J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995.*
2.	*K. J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.*
3.	*M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.*

17AEPE02	COMPUTER ARCHITECTURE	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the difference between pipeline and parallel processing concepts
- To study various types of processor architectures and the importance of scalable architectures
- To study Memory Optimization and Technique.
- To learn issues related to memory architecture.
- To study Memory Architectures

UNIT I	COMPUTER DESIGN AND PERFORMANCE MEASURES	9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures

UNIT II	PARALLEL PROCESSING, PIPELINING AND ILP	9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III	MEMORY HIERARCHY DESIGN	9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV	MULTIPROCESSORS	9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V	MULTI-CORE ARCHITECTURES	9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Have the basic fundamentals of computer design and measure the performance.
•	Understand pipelining and parallel processing
•	Explain design of memory hierarchies.
•	Assess Performance Issues and Synchronization issues.
•	Compare multicore architectures.
REFERENCES:	
1.	*D. E. Culler, J. P.Singh, "Parallel Computing Architecture: A hardware/ software approach", Morgan Kaufmann / Elsevier, 1997.*
2.	*D.Soudris, A. Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012.*
3.	*H. Briggs, "Computer Architecture and parallel processing", McGraw Hill, 1984.*
4.	*J.L. Hennessey and D. A. Patterson, "Computer Architecture – A quantitative approach", Morgan Kaufmann / Elsevier, 4th. edition, 2007.*
5.	*J. P. Hayes, "Computer Architecture and Organization", McGraw Hill,3rd Edition,2017.*
6.	*J.P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill ,2003.*
7.	*K. Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.*
8.	*W. Stallings, "Computer Organization and Architecture – Designing for Performance", Pearson Education, Seventh Edition, 2006.*

17AEPE03	VLSI DESIGN TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the principles of MOS transistor and CMOS inverter.
- To study the layout and stick diagram of combinational circuits.
- To study various latches and register in logic circuits.
- To classify different building blocks and architecture.
- To discuss various digital systems design.

UNIT I	MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II	COMBINATIONAL LOGIC CIRCUITS	9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III	SEQUENTIAL LOGIC CIRCUITS	9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

UNIT IV	ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES	9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V	INTERCONNECT AND CLOCKING STRATEGIES	9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Design digital systems using MOS transistor and invertors.
•	Able to learn layout, stick diagram in combinational logic circuits
•	Discuss various latches and registers in sequential circuits.
•	Discuss design methodology of arithmetic building block.
•	Analyze tradeoffs of the various circuit choices for each of the building block.
REFERENCES:	
1.	*J. Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010.*
2.	*J. Rabaey, A. Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Prentice Hall of India 2nd Edition, 2003.*
3.	*M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.*
4.	*N.Weste, K. Eshraghian, ," Principles of CMOS VLSI Design".,Addision Wesley, 2nd Edition, 1993.*

17AEPE04	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the basics of EMI
- Be familiar with EMI sources and problems.
- To understand solution methods in PCB.
- To discuss various measurement techniques for emission.
- To discuss various measurement techniques for immunity.

UNIT I	BASIC THEORY	9

Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II	COUPLING MECHANISM	9

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III	EMI MITIGATION TECHNIQUES	9

Working principle of Shielding and Murphy‟s Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV	STANDARD AND REGULATION	9

Need for Standards, Generic/General Standards for Residential and Industrial environment, Basic Standards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

UNIT V	EMI TEST METHODS AND INSTRUMENTATION	9

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks,

Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.	
	TOTAL : 45 PERIODS
OUTCOMES:	
•	Able to learn basic idea about EMI and EMC.
•	Discuss different coupling mechanism.
•	Discuss EMI mitigation techniques.
•	Identify Standards.
•	Compare EMI test methods.
REFERENCES:	
1.	*B. Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.*
2.	*C. Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience, 2006.*
3.	*D. Gerke and W. Kimmel, "EDN's Designer's Guide to Electromagnetic Compatibility", Elsevier Science & Technology Books, 2002.*
4.	*Dr K. L .Kaiser, "The Electromagnetic Compatibility Handbook", CRC Press, 2005.*
5.	*N.Violette , "Electromagnetic Compatibility", ,Published by Springer, 2013.*
6.	*D. R. J. White , "Electromagnetic Interference and Compatibility: Electrical noise and EMI specifications Volume 1 of A Handbook Series on Electromagnetic Interference and Compatibility", Publisher-Don white consultants Original from the University of Michigan Digitized 6 , 2007.*
7.	*H. W. Ott, "Electromagnetic Compatibility Engineering", John Wiley & Sons , Newyork,, 2009.*
8.	*V .P. Kodali, "Engineering Electromagnetic Compatibility", IEEE Press, Newyork, ,2001.*

PROFESSIONAL ELECTIVES (PE)

SEMESTER -II

ELECTIVE II

17AEPE05	CAD FOR VLSI	L	T	P	C
		3	0	0	3

BJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow
- To understand the concepts of various algorithms used for floor planning and routing techniques.
- To study hardware models for high level synthesis.

UNIT I	INTRODUCTION TO VLSI DESIGN FLOW	9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II	LAYOUT, PLACEMENT AND PARTITIONING	9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.

UNIT III	FLOOR PLANNING AND ROUTING	9

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV	SIMULATION AND LOGIC SYNTHESIS	9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V	HIGH LEVEL SYNTHESIS	9

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL : 45 PERIODS

OUTCOMES:	
•	To use the simulation techniques at various levels in VLSI design flow.
•	Discuss the layout design rules and various placement algorithms.
•	Discuss the concepts of floor planning and routing.
•	Outline high level synthesis.
•	Discuss VLSI design methodology and its design automation tools.
REFERENCES:	
1.	*N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, Third Edition, 2002.*
2.	*S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.*
3.	*S.M. Sait, H.Youssef, "VLSI Physical Design automation: Theory and Practice", World scientific, 1999.*
4.	*S.M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing, 1987.*

17AEPE06	NANOELECTRONICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn and understand basic concepts of Nano electronics.
- To know about electronic and photonic materials.
- To understand how transistor as Nano device.
- To gain knowledge about Nano Sensors.
- To understand various forms of nano devices.

UNIT I	SEMICONDUCTOR NANO DEVICES	9

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II	ELECTRONIC AND PHOTONIC MATERIALS	9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III	THERMAL SENSORS	9

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV	GAS SENSORS	9

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V	BIOSENSORS	9

Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Knowledge of various materials used in nano devices.
•	Able to design and simulate nano device.
•	Exposure to the different nano sensors.
•	Able to design and simulate nano sensors.
•	To familiarize with the present research front in Nanooelectronics and to be able to critically assess future trends.
REFERENCES:	
1.	*K.E. Drexler, "Nano systems", Wiley,1992.*
2.	*M.C. Petty, "Introduction to Molecular Electronics", Oxford University Press,1995.*
3.	*W. Ranier, "Nano Electronics and Information Technology", Wiley, Third Edition, 2012.*

17AEPE07	SENSORS AND MEASUREMENTS SYSTEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To know the static and dynamic characteristics of measurement systems.
- To study about the various types of sensors viz. Resistive, Reactive.
- To study about Self- generating sensors.
- To know the different types digital and semiconductor sensors.
- To study different types of actuators and their usage.

UNIT I	INTRODUCTION TO MEASUREMENT SYSTEMS	9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II	RESISTIVE AND REACTIVE SENSORS	9

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

UNIT III	SELF-GENERATING SENSORS	9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

UNIT IV	ACTUATOR CHARACTERISTICS AND APPLICATIONS	9

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V	DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS	9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions,

magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.	
	TOTAL : 45 PERIODS
OUTCOMES:	
•	Discuss measurement systems.
•	Knowledge about resistive and reactive sensors.
•	Discuss Self-generating sensors.
•	Analyze the characteristics of Actuators.
•	Evaluate digital sensors and semiconductor device sensors.
REFERENCES:	
1.	*A.M. Pawlak," Sensors and Actuators in Mechatronics Design and Applications", CRC Press, 2006.*
2.	*D. Johnson, "Process Control Instrumentation Technology", John Wiley and Sons, Eighth Edition, 2006.*
3.	*D.Patranabis, "Sensors and Transducers", TMH, Second Edition, 2003.*
4.	*E.O. Doeblin, "Measurement System : Applications and Design", McGraw Hill publications, Fifth Edition, 2007 .*
5.	*G.Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.*
6.	*H.K.P. Neubrat, "Instrument Transducers – An Introduction to Their Performance and Design", Oxford University Press, Second Edition.*
7.	*I.Sinclair, "Sensors and Transducers", Elsevier, 3rd Edition, 2011.*
8.	*J.Wilson , "Sensor Technology Handbook", Elsevier, First Edition, 2004.*
9.	*K. James, PC Interfacing and Data acquisition, Elsevier, First Edition.*
10.	*Ramon Pallás-Areny, John G. Webster, "Sensors and Signal Conditioning", 2nd edition, John Wiley and Sons, 2012.*
11.	*C.W. de Silva, "Sensors and Actuators: Control System Instrumentation", CRC Press, Second Edition, 2015.*

17AEPE08	MEMS AND NEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.
- To introduce various opportunities in the emerging field of MEMS.

UNIT I	OVERVIEW	9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II	MEMS FABRICATION TECHNOLOGIES	9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III	MICRO SENSORS	9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV	MICRO ACTUATORS	9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators. components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V	NANOSYSTEMS AND QUANTUM MECHANICS	9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Be familiar with the important concepts related to MEMS.
•	Outline MEMS fabrication technology.
•	Design of micro actuators.
•	Analyze the engineering mechanism of micro sensors.
•	Outline nano systems and Quantum mechanics.
REFERENCES:	
1.	*C.Liu, "Foundations of MEMS", Pearson education India limited, Second Edition, 2011.*
2.	*M.Madou, "Fundamentals of Microfabrication and NanoTechnology", CRC press, Third Edition, 2011.*
3.	*S.D. Senturia," Micro system Design", Kluwer Academic Publishers,2001*
4.	*S.E.Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.*
5.	*T.R.Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata McGraw Hill, First Edition, 2002*

SEMESTER- II

ELECTIVE III

17AEPE09	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

•	To give an exposure to the various DSP architectures and to develop applications using these processors.
•	Knowledge on digital signal processor basics.
•	Knowledge on third generation DSP Architecture.
•	Knowledge on programming skills.
•	Knowledge on advanced DSP architectures and some applications.

UNIT I	FUNDAMENTALS OF PROGRAMMABLE DSPs	9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II	SPECIAL FUNCTIONS	9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III	LINEAR PROGRAMMING	9

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV	LINEAR PROGRAMMING	9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V	ALGEBRAIC EQUATIONS	9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

	TOTAL : 45 PERIODS

OUTCOMES:	
•	Learn the architecture details and instruction sets of DSP.
•	Understand the special functions of DSP architecture and programming.
•	Interfacing of programmable DSP devices for system implementation.
•	Create application programs.
•	Evaluate features of DSP family processors.
REFERENCES:	
1.	*A.Singh and S. Srinivasan," Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx", Cengage Learning India Private Limited Delhi, 2012.*
2.	*B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, Second Edition, 2010.*
3.	*RulphChassaing, D.S.Reay, "Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK", A JOHN WILEY & SONS, INC., PUBLICATION, Second Edition, 2011.*
4.	*User guides Texas Instrumentation, Analog Devices, Motorola.*

17AEPE10	RF SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the principles of operation and design principles associated with the important blocks of RF Front end.
- To design RF amplifier.
- To study about the characteristics of oscillators, mixers.
- The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs.
- To study about the characteristics of PLL and frequency synthesizers.

UNIT I	CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS ANDARCHITECTURES	9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II	IMPEDANCE MATCHING AND AMPLIFIERS	9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III	FEEDBACK SYSTEMS AND POWER AMPLIFIERS	9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

UNIT IV	MIXERS AND OSCILLATORS	9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V	PLL AND FREQUENCY SYNTHESIZERS	9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Understand the specifications and architecture design of transceivers.
•	Knowledge of impedance matching networks and design of high frequency amplifiers.
•	Design of feedback systems and power amplifiers.
•	Knowledge of mixers and oscillators.
•	Design of PLL and Frequency synthesizers.
REFERENCES:	
1.	*B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, Second Edition, 2017.*
2.	*B.Razavi, "RF Microelectronics", Pearson Education, Second Edition, 2012.*
3.	*J.Crols, M.Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.*
4.	*Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/*
5.	*T.Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, Second Edition, 2004.*

17AEPE11	SPEECH SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study basic concepts of processing speech signals.
- To study and analyse various M-band filter-banks for audio coding.
- To understand audio coding based on transform coders.
- To study time and frequency domain speech processing methods
- To understand predictive analysis of speech.

UNIT I	MECHANICS OF SPEECH AND AUDIO	9

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II	TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS	9

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies.

UNIT III	AUDIO CODING AND TRANSFORM CODERS	9

Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder –Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding –Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization.

UNIT IV	TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING	9

Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT V	PREDICTIVE ANALYSIS OF SPEECH	9
Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin‟s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	Ability to understand the mechanism of speech signal processing.
•	Analysis of filter banks and transforms in time domain.
•	Evaluate audio coding and transform coders.
•	Discuss time and frequency domain methods for speech processing.
•	Ability to analyze predictive analysis of speech.

REFERENCES:

1.	*B.Gold and N.Morgan, "Speech and Audio Signal Processing", Wiley and Sons, Second Edition, 2011.*
2.	*L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech Signals", Prentice Hall, 1979.*
3.	*M.Kahrs, K.Brandenburg, "Applications of Digital Signal Processing to Audio And Acoustics", Kluwer Academic Publishers, 1998.*
4.	*U.Zölzer, "Digital Audio Signal Processing", John Wiley& sons Ltd , Second Edition, 2008.*

17AEPE12	SOLID STATE DEVICE MODELLING AND SIMULATION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study physics of MOSFET devices.
- To understand the concept of device modelling.
- To learn multistep method.
- To study mathematical techniques of device simulations.
- To study device simulations.

UNIT I	MOSFET DEVICE PHYSICS MOSFET	9

Capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II	DEVICE MODELLING	9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III	MULTISTEP METHODS	9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV	MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS	9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V	SIMULATION OF DEVICES	9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Able to understand the importance of MOS Capacitor and Small signal modelling.
•	Apply and determine the drift diffusion equation and stiff system equation.
•	Analyze circuits using parasitic BJT parameters and Newton Raphson method.
•	Modelling of MOS transistor using Schrodinger equation and Multistep methods.
•	Ability to do simulation to compute the characteristics of MOSFET devices.
REFERENCES:	
1.	*Arora, N., "MOSFET Modelling for VLSI Simulation", Cadence Design Systems, 2007.*
2.	*Chua, L.O. and Lin, P.M., "Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques", Prentice-Hall., 1975.*
3.	*Fjeldly, T., Yetterdal, T. and Shur, M., "Introduction to Device Modelling and Circuit Simulation", Wiley-Interscience., 1997.*
4.	*Grasser, T., "Advanced Device Modelling and Simulation", World Scientific Publishing Company., 2003.*
5.	*Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer- Verlag.,1984.*
6.	*T.Ytterdal, Y.Cheng and Tor A. FjeldlyWayne Wolf, "Device Modelling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd,2003.*

SEMESTER- III

ELECTIVE IV

17AEPE13	ADVANCED MICROPROCESSOR AND MICROCONTROLLER ARCHITECTURES	L	T	P	C
		3	0	0	3

OBJECTIVES:

•	To familiarize about the features, specification and features of modern microprocessors.
•	To gain knowledge about the architecture of Intel 32 and 64 bit microprocessors and salient features associated with them.
•	To familiarize about the features, specification and features of modern microcontrollers.
•	To gain knowledge about the 32 bit microcontrollers based on ARM and PIC32 architectures.
•	To study interfacing of microprocessor/microcontroller with the external peripheral.

UNIT I	FEATURES OF MODERN MICROPROCESSORS	9

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over clocking – integrated graphics processing - performance benchmarks.

UNIT II	HIGH PERFORMANCE CISC ARCHITECTURES	9

Introduction to IA 32 bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT III	HIGH PERFORMANCE RISC ARCHITECTURE – ARM	9

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3- stage pipeline ARM organization - ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles)

UNIT IV	FEATURES OF MODERN MICROCONTROLLER	9

Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces– Communication interfaces (SPI,I2C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces .

UNIT V	HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES	9
Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-M3 architecture		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	To explain the features and important specifications of modern microprocessors.
•	To explain the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures.
•	To explain the salient features RISC processors based on ARM architecture and different application profiles of ARM core.
•	To explain the features and important specifications of modern microcontrollers.
•	To explain about ARM – M3 architecture and its salient features.

REFERENCES:

1.	*Barry. B. Breg," The Intel Microprocessors" , PHI,2008.*
2.	*Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.*
3.	*Intel Inc, "Intel 64 and IA-32 Architectures Developer"s Manual", Volume-I, 2016*
4.	*J. Yiu, "The Definitive Guide to the ARM ® Cortex-M3", Newnes, 2010.*
5.	*S.Mueller, "Upgrading and Repairing PCs", 20th edition, Que.*
6.	*S.Furber, „" ARM System –On –Chip architecture "Addision Wesley , 2000.*
7.	*T. Martin, "The Designer"s Guide to the Cortex-M Processor Family", Newnes, 2013.*

17AEPE14	SYSTEM ON CHIP DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand what SOC is and what the difference between SOC and Embedded system.
- To understand system design methodology in SOC.
- To cover the basics of SOC design, hardware software co design and synthesis.
- To study different levels of SOC verification.
- To study testing of SOC.

UNIT I	INTRODUCTION	9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design.

UNIT II	SYSTEM LEVEL MODELLING	9

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples.

UNIT III	HARDWARE AND SOFTWARE CO -DESIGN	9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV	SYNTHESIS	9

System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling.

UNIT V	SOC VERIFICATION AND TESTING	9

SoC and IP integration, Verification: Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism.

TOTAL : 45 PERIODS

OUTCOMES:

- Analyse algorithms and architecture of hardware software in order to optimise the system based on requirements and implementation constraints.
- Model and specify systems at high level of abstraction.

•	Understand hardware, software and interface synthesis.
•	Appreciate the co-design approach and virtual platform models.
•	Ability to do SOC verification and testing.

REFERENCES:

1.	*D. Black, J. Donovan, "SystemC: From the Ground Up", Springer, Second Edition, 2010.*
2.	*D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, "Embedded System Design: Modeling, Synthesis, Verification", Springer, 2009*
3.	*H.Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.*
4.	*J.Ho¨ ller, V.Tsiatsis , C.Mulligan, Stamatis , Karnouskos, S.Avesand. D.Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.*
5.	*O.Hersent, D.Boswarthick, O.Elloumi , "The Internet of Things – Key applications and Protocols", Wiley,Second Edition, 2012.*
6.	*Hoi-junyoo, K.Lee, J.Kyoungkim, "Low power NoC for high performance SoC design", CRC press, 2008.*
7.	*M. L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", Springer, 2005*
8.	*M. Abramovici, M. Breuer, and A. Friedman, "Digital System Testing and Testable Design", IEEE Press, 1994.*
9.	*P. Marwedel, G. De Micheli ,"Synthesis and Optimization of Digital Circuits" Springer, 2003.*
10.	*P.Rashinkar, P.Paterson and L.Singh, "System-on-a chip verification: Methodology and techniques", Kluwer Academic Publishers, 2002.*
11.	*T. Noergaard, "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Newnes, Second Edition, 2012.*
12.	*V.K. Madisetti, C.Arpikanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2005.*
13.	*Y.L Steve, Lin, "Essential Issues in SOC Design Designing Complex Systems-on-Chip", Springer, 2006.*

17AEPE15	ROBOTICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics.
- To understand perception in robotics.
- To understand mobile robot localization.
- To understand mobile robot mapping.
- To understand robot planning and navigation.

UNIT I	LOCOMOTION AND KINEMATICS	9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT II	ROBOT PERCEPTION	9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data

UNIT III	MOBILE ROBOT LOCALIZATION	9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments

UNIT IV	MOBILE ROBOT MAPPING	9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM –extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fast SLAM algorithm.

UNIT V	PLANNING AND NAVIGATION	9

Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms.

TOTAL : 45 PERIODS

OUTCOMES:

- Explain robot locomotion.
- Apply kinematics models and constraints.
- Implement vision algorithms for robotics.

•	Implement robot localization techniques.
•	Implement robot mapping techniques.
•	Implement SLAM algorithms.
•	Understand the algorithms for planning and navigation in robotics.

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2.	*H.Choset et al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", A Bradford Book, 2005.*
3.	*M.J. Mataric, "The Robotics Primer", MIT Press, 2007.*
4.	*R.Seigwart, I.R.Nourbakhsh, and D.Scaramuzza, "Introduction to autonomous mobile robots", Second Edition, MIT Press, 2011.*
5.	*S.Thrun, W.Burgard, and D.Fox, "Probabilistic Robotics", MIT Press, 2005.*

17AEPE16	PHYSICAL DESIGN OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the physical design concepts such as layout rules, circuit abstraction, layout methodologies and packaging.
- To study placement of design using top down approach.
- To study different approaches of routing.
- To study performance issues in circuit layout.
- To study 1D compaction and 2D compaction.

UNIT I	INTRODUCTION TO VLSI TECHNOLOGY	9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms.

UNIT II	PLACEMENT USING TOP-DOWN APPROACH	9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III	ROUTING USING TOP DOWN APPROACH	9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs.

UNIT IV	PERFORMANCE ISSUES IN CIRCUIT LAYOUT	9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

UNIT V	SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION	9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Exposure to the layout design methodologies.
•	Analyze placement and routing techniques.
•	Analyze performance issues in circuit layout.
•	Analyze techniques of single layer routing, cell generation and compaction.
•	Outline 1D compaction and 2D compaction.
REFERENCES:	
1.	*P.M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.*
2.	*Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill Int. Edition, 1995*
3.	*Michael S. Smith, "Application Specific Integrated Circuits", Addison-Wesley,1997.*
4.	*S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.*

17AEPE17	HIGH PERFORMANCE NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networks.
- To study the types of VPN and tunnelling protocols for security.
- To learn about network security in many layers and network management.
- To study advanced network concepts.
- To discuss traffic modelling.

UNIT I	INTRODUCTION	9

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.

UNIT II	MULTIMEDIA NETWORKING APPLICATIONS	9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III	ADVANCED NETWORKS CONCEPTS	9

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, and MPLS based VPN, overlay networks- P2P connections.

UNIT IV	TRAFFIC MODELLING	9

Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

UNIT V	NETWORK SECURITY AND MANAGEMENT	9

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL : 45 PERIODS

OUTCOMES:

- Analyze scheduling and policing mechanism and protocols for real time interactive applications.
- Discuss advanced networks concepts.

•	Outline traffic modelling.
•	Evaluate network security and management.
•	Evaluate network performance.

REFERENCES:

1.	*A.Kumar, D. M Anjunath, J.Kuri, "Communication Networking", Morgan Kaufmann Publishers, 1st edition, 2004.*
2.	*F.Halsall and L.G Kulkarni, "Computer Networking and the Internet", fifth edition, Pearson education 2006.*
3.	*H.Gurle & Petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.*
4.	*J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.*
5.	*L.l.Peterson & B.S.David, "Computer Networks: A System Approach", Morgan Kaufmann Publishers, Fifth Edition, 2011.*
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7.	*N.F.Mir, "Computer and Communication Networks", Second Edition, Prentice Hall of India, 2014.*
8.	*W..J. Varatya, "High performance communication network", Morgan Kauffman – Harcourt Asia Pvt. Ltd, 2nd Edition, 2000.*

SEMESTER- III

ELECTIVE V

17AEPE18	PATTERN RECOGNITION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn about supervised and unsupervised pattern classifiers
- To learn about different clustering methods.
- To familiarize about different feature extraction techniques
- To explore the role of Hidden Marko model and SVM in pattern recognition
- To understand the application of Fuzzy logic and genetic algorithms for pattern classifier

UNIT I	PATTERN CLASSIFIER	9

Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT II	CLUSTERING	9

Clustering for unsupervised learning and classification–Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III	FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION	9

Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions

UNIT IV	HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE	9

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection.

UNIT V	RECENT ADVANCES	9

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

	TOTAL : 45 PERIODS

OUTCOMES:

•	Differentiate between supervised and unsupervised classifiers
•	Classify the data and identify the patterns.
•	Apply the concepts of clustering
•	Extract feature set and select the features from given data set.
•	Apply fuzzy logic and genetic algorithms for classification problems

REFERENCES:

1.	*Andrew Webb, "Stastical Pattern Recognition", Arnold publishers, London,1999*
2.	*C.M.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.*
3.	*M. Narasimha Murthy and V. Susheela Devi, "Pattern Recognition", Springer 2011.*
4.	*Menahem Friedman , Abraham Kandel, "Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches", World Scientific publishing Co. Ltd, 2000.*
5.	*Robert J.Schalkoff, "Pattern Recognition Statistical, Structural and Neural Approaches", John Wiley & Sons Inc., New York, 1992.*
6.	*R.O.Duda, P.E.Hart and D.G.Stork, "Pattern Classification", John Wiley, 2001*
7.	*S.Theodoridis and K.Koutroumbas, "Pattern Recognition", 4th Ed., Academic Press. 2009.*

17AEPE19	SECURE COMPUTING SYSTEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn different computer security mechanism and management techniques.
- To gain knowledge about computer hardware security.
- To apply programming knowledge in hardware.
- To learn advanced computer architecture.
- To learn the equation and theory those are used in network security.

UNIT I	COMPUTER SECURITY AND MANAGEMENT	9

Overview of Computer Security, Threats, Malware, Vulnerabilities, Authentication, Access Control, Security Management Models, Security Management Practices, Protection Mechanisms, Legal aspects of security, Ethical Hacking.

UNIT II	HARDWARE SECURITY	9

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Countermeasures of Side Channel Attack, Secure Hardware Intellectual Properties, Physically Unclonable Functions(PUFs), Secure PUF.

UNIT III	ASSEMBLY AND OPERATING SYSTEMS SECURITY	9

Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions

UNIT IV	ADVANCED COMPUTER ARCHITECTURE	9

Security aspects : Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization

UNIT V	NETWORK AND WEBSECURITY	9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL : 45 PERIODS

OUTCOMES:	
•	Aware of Security aspects
•	Able to appreciate security in hardware, OS and it future need
•	Learn security issues in various types of computing networks
•	Learn advanced computer architecture.
•	Outline the equation and theory which are used in web security.
REFERENCES:	
1.	*Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", Fourth Edition, Pearson Education, 2007*
2.	*Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design Threats and Safeguards", CRC Press, 2015*
3.	*Michael Whitman, Herbert J. Mattord, "Management of Information Security", Third Edition, Course Technology, 2010*
4.	*Shuangbao Wang, Robert S.Ledley, Computer Architecture and Security, Wiley, 2013*
5.	*William Stallings, "Network Security Essentials, Applications and Standards", Dorling Kindersley I P Ltd, Delhi, 2008.*
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7.	*Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design Threats and Safeguards", CRC Press, 2015*

17AEPE20	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics
- To learn non-ideal effects of transmission lines.
- To gain knowledge about clock distribution and clock oscillators.
- To analyze the power consideration in digital circuits.

UNIT I	SIGNAL PROPAGATION ON TRANSMISSION LINES	9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II	MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK	9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

UNIT III	NON-IDEAL EFFECTS	9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

UNIT IV	POWER CONSIDERATIONS AND SYSTEM DESIGN	9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V	CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.matrix layout- 1D compaction- 2D compaction.

	TOTAL : 45 PERIODS
OUTCOMES:	
•	Ability to identify sources affecting the speed of digital circuits
•	Able to improve the signal transmission characteristics.
•	Understand clock distribution and clock oscillators.
•	Learn Multi-conductor transmission line and crosstalk.
•	Learn Power consideration and system design for high speed design.
REFERENCES:	
1.	*Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003*
2.	*Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.*
3.	*H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.*
4.	*S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.*

17AEPE21	WIRELESS ADHOC AND SENSOR NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study the ADHOC networks and its protocols
- To implement the designing of multicast routing and security
- To study the Challenges in QOS and power management schemes
- To study the sensor networks and MAC protocols
- To explore the sensor networks and operating systems

UNIT I	MAC & TCP IN AD HOC NETWORKS	9

Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration- Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT II	ROUTING IN AD HOC NETWORKS	9

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches- Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT III	MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS	9

Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support.

UNIT IV	SENSOR MANAGEMENT	9

Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.

UNIT V	SECURITY IN AD HOC AND SENSOR NETWORKS	9
Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defence against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.		
	TOTAL : 45 PERIODS	

OUTCOMES:

•	Identify different issues in wireless ad hoc and sensor networks.
•	Analyze protocols developed for ad hoc and sensor networks.
•	Outline different routing techniques and challenges in providing Qos.
•	Identify and address the security threats in ad hoc and sensor networks.
•	Establish a Sensor network environment for different type of applications.

REFERENCES:

1.	*Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition), World Scientific Publishing, 2011*
2.	*C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.*
3.	*C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2002.*
4.	*Erdal Çayırcı , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.*
5.	*Holger Karl, Andreas willig, Protocols and Architectures for Wireless Sensor Networks, John Wiley & Sons, Inc .2005.*
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7.	*Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley and Sons, 2010.*