GOVERNMENT COLLEGE OF ENGINEERING

BARGUR, KRISHNAGIRI – 635104

(An Autonomous Institution – Affiliated to Anna University, Chennai)

REGULATION 2025

CURRICULUM AND SYLLABUS

M.E.

APPLIED ELECTRONICS

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
AUTONOMOUS
Regulation – 2025

Curriculum for Full Time – M.E. –Applied Electronics
from the Academic Year 2025-2026 onwards

Programme Outcomes (PO):

PO1 Ability to acquire in-depth knowledge in the field of Electronics with a ability to evaluate and analyze the existing knowledge for enhancement.

PO2 Ability to analyze critical complex engineering problems and provide solutions through research.

PO3 Ability to think latterly and solve engineering problems optimally considering public health and safety, cultural and societal factors in the core areas.

PO4 Ability to extract information pertinent to challenging problems through literature survey and by appropriate research methodologies, techniques and tools to the development of technological knowledge.

PO5 Ability to select, learn and apply appropriate techniques, resources and modern engineering tools to complex engineering activities with an understanding of limitations

PO6 Ability to understand group dynamics, recognize opportunities and contribute positively to multidisciplinary work to achieve common goals for further learning.

PO7 Ability to demonstrate engineering principles and apply the same to manage projects efficiently as a team after considering economical and financial factors.

PO8 Ability to communicate with engineering community and society regarding complex engineering activities effectively through reports, design documentation and presentation.

PO9 Ability to encage with commitment in life-long learning independently to improve knowledge and competence.

PO10 Ability to acquire professional and intellectual integrity, professional code and contact, ethics of research and scholarship by considering the research outcomes to the community for sustainable development of society.

PO11 Ability to observe and examine critically the outcomes and make corrective measures, and learn from mistakes without depending on external feedback.

Programme Specific Outcomes (PSO):

PSO1 To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, communications, digital system design, embedded systems and VLSI design.

PSO2 To develop electronic systems using modern engineering hardware and software tools.

PSO3 To work professionally and ethically in applied electronics and allied areas.

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M.E. APPLIED ELECTRONICS

ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULUM DESIGN – REGULATION 2025
CREDIT SUMMARY

Name of the PG Programme : **M.E – APPLIED ELECTRONICS**

Credit Summary

S. No	Subject Category / Semester	1	2	3	4	Total Credits	Credits as per AICTE	Credits as per Anna University
1.	FC	4				4	0	4
2.	PC	15	14			29	20	31
3.	PE	3	6	6		15	15	16
4.	OE			3		3	3	3
5.	EEC		1	8	12	21	28	19
6.	AC/ (MC)			2		2	2	2
Total		22	21	19	12	74	68	75

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REGULATIONS 2025

SEMESTER I

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
THEORY								
1	25AEFC01	Mathematical Foundations for Electronics Engineers	FC	4	4	0	0	4
2	25AEPC02	Advanced Digital System Design	PC	3	3	0	0	3
3	25AEPC03	Advanced Digital Signal Processing	PC	4	4	0	0	4
4	25AEPC04	Embedded System Design	PC	3	3	0	0	3
5	25AEPC05	Modern Communication Techniques	PC	3	3	0	0	3
6	25ZMC001	Research Methodology and IPR	MC	2	2	0	0	2
7		Audit Course - I	AC	2	2	0	0	0
PRACTICALS								
8	25AEPC06	Electronic System Design Laboratory -I	PC	4	0	0	4	2
TOTAL				**25**	**21**	**0**	**4**	**21**

SEMESTER II

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
THEORY								
1	25AEPC07	Soft Computing and Optimization Techniques	PC	3	3	0	0	3
2	25AEPC08	VLSI System Design	PC	3	3	0	0	3
3	25AEPC09	Digital Image Processing	PC	3	3	0	0	3
4	25AEPC10	Internet of Things	PC	3	3	0	0	3
5		Professional Elective - I	PE	3	3	0	0	3
6		Professional Elective - II	PE	3	3	0	0	3
7		Audit Course - II	AC	2	2	0	0	0
PRACTICALS								
8	25AEPC11	Electronic System Design Laboratory-II	PC	4	0	0	4	2
9	25AEEE12	Term Paper Writing And Seminar	EEC	2	0	0	2	1
TOTAL				**26**	**20**	**0**	**6**	**21**

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SEMESTER III

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
THEORY								
1		Open Elective -I	OEC	3	3	0	0	3
2		Professional Elective - III	PE	3	3	0	0	3
3		Professional Elective - IV	PE	3	3	0	0	3
4		Professional Elective - V	PE	3	3	0	0	3
PRACTICALS								
5	25PEEE14	Internship(4 Weeks)	EEC	0	0	0	0	2
6	25PEEE15	Dissertation-I	EEC	12	0	0	12	6
			TOTAL	**24**	**12**	**0**	**12**	**20**

SEMESTER IV

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
PRACTICALS								
1	25PEEE16	Dissertation - II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL CREDITS: 74

MANDATORY COURSE (To be studied in any semester from I to III)

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
1	25ZMC001	Research methodology and IPR	MC	2	2	0	0	2
			TOTAL	2	2	0	0	2

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PROFESSIONAL ELECTIVE COURSES

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
1.	25AEPE01	Digital Control Engineering	PE	3	3	0	0	3
2.	25AEPE02	Computer Architecture	PE	3	3	0	0	3
3.	25AEPE03	Digital VLSI design	PE	3	3	0	0	3
4.	25AEPE04	EMI and EMC in System Design	PE	3	3	0	0	3
5.	25AEPE05	CAD for VLSI	PE	3	3	0	0	3
6.	25AEPE06	Nano electronics	PE	3	3	0	0	3
7.	25AEPE07	Sensors and Signal Conditioning	PE	3	3	0	0	3
8.	25AEPE08	MEMS and NEMS	PE	3	3	0	0	3
9.	25AEPE09	DSP Integrated Circuits	PE	3	3	0	0	3
10.	25AEPE10	RF System Design	PE	3	3	0	0	3
11.	25AEPE11	Speech Signal Processing	PE	3	3	0	0	3
12.	25AEPE12	Solid State Device Modeling and Simulation	PE	3	3	0	0	3
13.	25AEPE13	Advanced Microprocessor and Microcontroller Architecture	PE	3	3	0	0	3
14.	25AEPE14	System on Chip	PE	3	3	0	0	3
15.	25AEPE15	Robotics and Intelligent Systems	PE	3	3	0	0	3
16.	25AEPE16	Physical Design of VLSI Circuits	PE	3	3	0	0	3
17.	25AEPE17	High Performance Networks	PE	3	3	0	0	3
18.	25AEPE18	Pattern Recognition	PE	3	3	0	0	3
19.	25AEPE19	Secure Computing Systems	PE	3	3	0	0	3
20.	25AEPE20	Signal Integrity for High Speed Design	PE	3	3	0	0	3
21.	25AEPE21	Wireless Ad-hoc and Sensor Networks	PE	3	3	0	0	3
22.	25AEPE22	Hardware–Software Co-design	PE	3	3	0	0	3
23.	25AEPE23	Programming Languages for Embedded Software	PE	3	3	0	0	3

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OPEN ELECTIVES (OFFERED TO THE OTHER DEPARTMENTS)

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
1	25AEOE01	Automotive Electronic Systems	OEC	3	3	0	0	3
2	25AEOE02	Sensors and Actuators	OEC	3	3	0	0	3
3	25AEOE03	PCB Design	OEC	3	3	0	0	3
4	25AEOE04	Micro Electro Mechanical Systems	OEC	3	3	0	0	3

LIST OF AUDIT COURSES

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
1	25ZAC001	Disaster Management	AC	2	2	0	0	0
2	25ZAC002	English for Research Paper Writing	AC	2	2	0	0	0
3	25ZAC003	Value Education	AC	2	2	0	0	0
4	25ZAC004	Pedagogy Studies	AC	2	2	0	0	0
5	25ZAC005	Stress Management by Yoga	AC	2	2	0	0	0
6	25ZAC006	Personality Development through Life Enlightenment Skills	AC	2	2	0	0	0
7	25ZAC007	Electronic Waste Management	AC	2	2	0	0	0

LIST OF PROFESSIONAL CORE COURSES (PCC)

SI No	Course Code	Course Name	Course Category	L	T	P	C
1	25AEPC02	Advanced Digital System Design	PC	3	0	0	3
2	25AEPC03	Advanced Digital Signal Processing	PC	4	0	0	4
3	25AEPC04	Embedded System Design	PC	3	0	0	3
4	25AEPC05	Modern communication techniques	PC	3	0	0	3
5	25AEPC06	Electronic System Design Laboratory-I	PC	0	0	4	2
6	25AEPC07	Soft Computing and Optimization Techniques	PC	3	0	0	3
7	25AEPC08	VLSI System Design	PC	3	0	0	3
8	25AEPC09	Digital Image Processing	PC	3	0	0	3
9	25AEPC10	Internet of Things	PC	3	0	0	3
10	25AEPC11	Electronic System Design Laboratory-II	PC	0	0	4	2

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LIST OF EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SI No	Course Code	Course Name	Course Category	Contact Hours	L	T	P	C
1	25AEEE12	Term Paper Writing and Seminar	EEC	2	0	0	2	1
2	25AEEE14	Internship	EEC		0	0	0	2
3	25AEEE15	Dissertation-I	EEC	12	0	0	0	6
4	25AEEE16	Dissertation- II	EEC	24	0	0	24	12

LIST OF FOUNDATIONAL COURSES (FC)

SI No	Course Code	Course Name	Course Category	L	T	P	C
1	25AEFC01	Mathematical Foundations for Electronics Engineers	FC	4	0	0	4

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SEMESTER-I

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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Subject Code	**25AEFC01**	**Subject Title**	**MATHEMATICAL FOUNDATIONS FOR ELECTRONICS ENGINEERS**
Category	FC	**L-T-P-C**	4-0-0-4
Regulation	2025	**Semester**	I
Prerequisites	Logical reasoning and analytical problem-solving skills		

OBJECTIVES:

To develop the use of matrix algebra techniques which is needed by engineers for practical applications. To learn fuzzy logic, dynamic programming and queuing models to apply in real world problems.

Course Content:

FUZZY LOGIC (12 HOURS)

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

MATRIX THEORY (12 HOURS)

Some important matrix factorizations - Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization – Least squares method - Singular value decomposition - - To eplitz matrices and someapplications.

ONE DIMENSIONAL RANDOM VARIABLES (12 HOURS)

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

DYNAMIC PROGRAMMING (12 HOURS)

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

QUEUEING MODELS (12 HOURS)

Poisson Process – Markovian queues – Single and multi-server models – Little's formula – Machine interference model – Steadystate analysis – Self-service queue.

TOTAL :60 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of classical logic, multivalued logic, fuzzy sets, fuzzy propositions, and fuzzy quantifiers used in intelligent decision-making systems.	**L2**	**PO1**
CO2	Apply advanced matrix algebra techniques, including matrix factorizations, generalized eigenvectors, QR decomposition, least squares, singular value decomposition, and Toeplitz matrices to solve engineering problems.	**L3**	**PO1, PO2**
CO3	Apply dynamic programming principles, including forward and backward recursion, to formulate and solve optimization problems encountered in engineering applications.	**L3**	**PO2, PO3, PO5**

CO4	Analyze one-dimensional random variables and probability distributions by evaluating probability functions, moments, moment generating functions, and engineering applications.	**L4**	**PO1, PO2, PO4**
CO5	Evaluate queueing systems using Poisson processes, Markovian queue models, Little's formula, and steady-state analysis to solve real-world service and communication system problems.	**L5**	**PO2, PO4, PO5**

REFERENCES:

1. *Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.*
2. *George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications",Prentice Hall of India Pvt. Ltd., 1997.*
3. *Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of QueueingTheory", 4th Edition, John Wiley, 2014.*
4. *Johnson, R.A., Miller, I and Freund J., "Miller and Freund"s Probability and Statistics forEngineers", Pearson Education, Asia, 8th Edition, 2015.*
5. *Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia,NewDelhi,2016.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	2	2	2	-	3	-	-	-	-	-	-	2	3
CO2	-	2	2	2	-	3	-	-	-	-	-	-	2	3
CO3	-	2	2	2	-	3	-	-	-	-	-	-	2	3
CO4	-	2	2	2	-	3	-	-	-	-	-	-	2	3
CO5	-	2	2	2	-	3	-	-	-	-	-	-	2	3
25AEFC01	-	2	2	2	-	3	-	-	-	-	-	-	2	3

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	25AEPC02	Subject Title	ADVANCED DIGITAL SYSTEM DESIGN
Category	PC	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I
Prerequisites	Flip-Flops, Registers, Counters, and Finite State Machines		

OBJECTIVES:

- Introduce methods to analyze and design synchronous and asynchronous sequential circuit
- Introduce the architecture of programmable device
- Introduce design and implementation of digital circuits using programming tools

SEQUENTIAL CIRCUIT DESIGN (9HOURS)

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chartand realization using ASM.

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9HOURS)

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition tableand problems in transition table- design of synchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9HOURS)

Fault table method-path sensitization method – Boolean difference method-D algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test.

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9HOURS)

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL –Realizationof finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 400

SYSTEM DESIGN USING VERILOG (9HOURS)

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators for Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench -Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL :45 PERIODS

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Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of synchronous and asynchronous sequential circuits, state models, ASM charts, and programmable logic devices.	L2	PO1
CO2	Apply state reduction, state assignment, hazard analysis, and finite state machine design techniques to develop sequential digital circuits.	L3	PO1, PO2, PO3
CO3	Analyze digital systems using fault diagnosis algorithms, testability techniques, and Design for Testability (DFT) methods.	L4	PO2, PO4
CO4	Evaluate programmable logic device architectures and select suitable FPGA/PLA/PAL implementations for digital system applications.	L5	PO2, PO3, PO5
CO5	Design, implement, synthesize, and verify combinational and sequential digital systems using Verilog HDL and modern EDA tools.	L6	PO3, PO5

REFERENCES:

1. *Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004*
2. *M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, PrenticeHall, 1999.*
3. *M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.*
4. *Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001*
5. *Parag K.Lala "Digital system Design using PLD" B S Publications,2003*
6. *Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002*
7. *S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**2**	**-**
CO2	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**3**	**2**	**-**
CO3	**3**	**2**	**2**	**-**	**-**	**2**	**-**	**-**	**-**	**1**	**1**	**3**	**2**	**-**
CO4	**3**	**3**	**2**	**-**	**-**	**2**	**-**	**-**	**-**	**2**	**-**	**3**	**2**	**-**
CO5	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**3**	**2**	**-**
25AEPC02	**3**	**3**	**2**	**-**	**-**	**2**	**-**	**-**	**-**	**2**	**1**	**3**	**2**	**-**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	25AEPC03	**Subject Title**	ADVANCED DIGITAL SIGNAL PROCESSING
Category	PC	**L-T-P-C**	4-0-0-4
Regulation	2025	**Semester**	I
Prerequisites	Digital Signal Processing fundamentals , Engineering Mathematics		

OBJECTIVES:

- To introduce the basics of random signal processing and spectral estimation
- To understand the concepts of estimation and prediction of non-stationary signals.
- To learn about adaptive filtering and multirate signal processing.

DISCRETE RANDOM SIGNAL PROCESSING (12 HOURS)

Discrete Random Processes – Ensemble averages -Wide sense stationary process –Auto- correlation and Auto-covariance matrices - Properties – Parseval's Theorem -Weiner Khintchine relation - Power spectral density – Filtering random process, Spectral Factorization -White noise -Simulation of uniformly distributed/Gaussian distributed white noise – Simulation of Sine wave mixed with Additive White Gaussian Noise.

SPECTRUM ESTIMATION (12 HOURS)

Bias and Consistency of estimators - Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysis of estimators –Periodogram–Modified Periodogram, Barlett method - Welch estimation, Blackman Tukey method. Parametric methods: Model based approach - AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walkerequations, Solutions using Durbin's algorithm.

LINEAR ESTIMATION AND PREDICTION (12 HOURS)

Linear prediction – Forward prediction and Backward prediction– Levinson Durbin recursion algorithm - Wiener filter - FIR Wiener filter- Filtering and linear prediction, non-causal and causal IIR Wiener filters – Discrete Kalman filter.

ADAPTIVE FILTERS (12 HOURS)

FIR Adaptive filters - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS – Sliding window RLS.

MULTIRATE DIGITAL SIGNAL PROCESSING (12 HOURS)

Mathematical description of change of sampling rate – Interpolation and Decimation- Decimation by an integer factor – Interpolation by an integer factor – Sampling rate conversion by a rational factor –Filter implementation for sampling rate conversion- direct form FIR structures, Polyphase filter structures, time variant structures – Multistage implementation of multirate system.

TOTAL :60 PERIODS

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Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	POs Mapped
CO1	Understand the fundamentals of discrete random signal processing, random processes, power spectral density, and random signal simulation.	**L2**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO2	Analyze spectrum estimation techniques using non-parametric and parametric methods for finite-duration signals.	**L4**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO3	Apply linear estimation and prediction techniques including Wiener filters, Levinson-Durbin recursion, and Kalman filters.	**L3**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO4	Evaluate and design adaptive filtering algorithms such as LMS and RLS for signal processing applications.	**L5**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO5	Design multirate digital signal processing systems using interpolation, decimation, sampling-rate conversion, and polyphase filter structures.	**L6**	**PO1, PO2, PO4, PO5, PO7, PO9**

REFERENCES:

1. *Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wileyand Sons Inc., New York,*
2. *2006.*
3. *John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall ofIndia, New Delhi,2005.*
4. *P. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1992.*
5. *S. Kay," Modern spectrum Estimation theory and application", Prentice Hall,Englehood Cliffs,NJ1988.*
6. *Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986*
7. *Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	**2**	**2**	**-**	**1**	**1**	**-**	**2**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO2	**2**	**2**	**-**	**2**	**1**	**-**	**2**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO3	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO4	**2**	**2**	**-**	**2**	**2**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**2**	**1**
CO5	**2**	**2**	**-**	**2**	**2**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**2**	**1**
25AEPC03	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**1**	**1**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

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GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	**25AEPC04**	**Subject Title**	**EMBEDDED SYSTEM DESIGN**
Category	PC	**L-T-P-C**	3-0-0-3
Regulation	2025	**Semester**	I
Prerequisites	Computer Organization and Architecture, Fundamentals of Operating Systems		

OBJECTIVES:

- To learn the design challenges about embedded system.
- To learn the design challenges about embedded system.
- To understand different state machine and process models.

EMBEDDED SYSTEM OVERVIEW (9 HOURS)

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT- Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors

GENERAL AND SINGLE PURPOSE PROCESSOR (9 HOURS)

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters andwatchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

BUS STRUCTURES (9 HOURS)

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O,Arbitration,Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

STATE MACHINE AND CONCURRENTPROCESS MODELS (9 HOURS)

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification: Hardware/Software Co- Simulation, Reuse: Intellectual Property Cores, Design Process Models.

EMBEDDED SOFTWARE DEVELOPMENTTOOLS AND RTOS (9 HOURS)

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems –emulation anddebugging techniques – RTOS – System design using RTOS.

TOTAL:45PERIODS

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of embedded systems, design challenges, optimization metrics, and design methodology.	**L2**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO2	Apply the concepts of processor architecture, microcontrollers, memory organization, and embedded peripherals in embedded system design.	**L3**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO3	Analyze bus architectures, interfacing techniques, and communication protocols used in embedded systems.	**L4**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO4	Evaluate state machine models, concurrent process models, synchronization techniques, and embedded system design methodologies for real-time applications.	**L5**	**PO1, PO2, PO4, PO5, PO7, PO9**
CO5	Design embedded software solutions using development tools, debugging techniques, kernel porting, and RTOS for embedded applications.	**L6**	**PO1, PO2, PO4, PO5, PO7, PO9**

REFERENCES:

1. *Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embeddedsystems", 3rd*
2. *Edition 1999, Pearson Education.*
3. *Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet",PearsonEducation, 2002.*
4. *Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley &sons,2002.*
5. *Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.*

COURSEARTICULATIONMATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	**2**	**2**	**-**	**1**	**1**	**-**	**2**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO2	**2**	**2**	**-**	**2**	**1**	**-**	**2**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO3	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**-**	**1**
CO4	**2**	**2**	**-**	**2**	**2**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**2**	**1**
CO5	**2**	**2**	**-**	**2**	**2**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**2**	**1**
25AEPC04	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**-**	**1**	**-**	**-**	**2**	**1**	**1**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	**25AEPC05**	**Subject Title**	**MODERN COMMUNICATION TECHNIQUES**
Category	PC	**L-T-P-C**	3-0-0-3
Regulation	2025	**Semester**	I
Prerequisites	Probability Theory and Random Processes, Analog and Digital Communication		

POWER SPECTRUM AND COMMUNICATIONOVER MEMORYLESS CHANNEL(9 HOURS)

PSD of a Synchronous Data Pulse Stream – M–ary Markov source – Convolutionally Coded Modulation –Continuous Phase Modulation – Scalar and Vector Communication over Memory less Channel – Detection Criteria.

COHERENT AND NON –COHERENTCOMMUNICATION (9 HOURS)

Coherent Receivers – Optimum Receivers in WGN – IQ Modulation & Demodulation – Non– Coherent receivers in Random Phase Channels – M–FSK Receivers – Rayleigh and Rician Channels – Partially Coherent Receivers – DPSK – M –PSK – M –DPSK – BER Performance Analysis.

BANDLIMITED CHANNELS AND DIGITALMODULATIONS (9 HOURS)

Eye pattern – Demodulation in the presence of ISI and AWGN – Equalization techniques – IQ modulations – QPSK – QAM – QBOM – BER Performance Analysis – Continuous Phase Modulation – CPFM – CPFSK – MSK – OFDM

BLOCK CODED DIGITAL COMMUNICATION (9 HOURS)

Architecture and Performance – Binary Block Codes – Orthogonal – Bi–orthogonal – Trans– orthogonal – Shannon's Channel Coding Theorem – Channel Capacity – Matched Filter –Concepts of Spread Spectrum Communication – Coded BPSK and DPSK Demodulators – Linear Block Codes – Hamming– Golay Cyclic – BCH – Reed– Solomon Codes

CONVOLUTIONAL CODED DIGITALCOMMUNICATION (9 HOURS)

Representation of Codes using Polynomial – State Diagram – Tree Diagram and Trellis Diagram – Decoding Techniques using Maximum Likelihood – Viterbi Algorithm – Sequential and Threshold methods – Error probability performance for BPSK and Viterbi Algorithm – Turbo Coding

TOTAL:45PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the power spectral density, communication over memoryless channels, and detection criteria used in digital communication systems.	L2	PO1, PO2, PO4, PO5, PO6, PO9, PO11
CO2	Apply coherent and non-coherent receiver techniques to evaluate the performance of digital communication systems over fading channels.	L3	PO1, PO2, PO4, PO5, PO6, PO9, PO11
CO3	Analyze equalization techniques and digital modulation schemes for communication over band-limited channels.	L4	PO1, PO2, PO4, PO5, PO6, PO9, PO11
CO4	Evaluate the performance of block coding techniques and spread spectrum communication for reliable data transmission.	L5	PO1, PO2, PO4, PO5, PO6, PO9, PO11
CO5	Design convolutional coding systems and implement decoding techniques such as the Viterbi algorithm and Turbo codes for error control applications.	L6	PO1, PO2, PO4, PO5, PO6, PO9, PO11

REFERENCES:

1. *Simon M. K., Hinedi S. M. and Lindsey W. C., "Digital Communication Techniques,Signaling and*
2. *Detection", Prentice Hall India, 1995.*
3. *Simon Haykin, "Digital communications", John Wiley and Sons, 1998.*
4. *John G. Proakis, "Digital Communication", Fifth Edition, Mc Graw Hill Publication,2008.*
5. *Bernard Sklar, "Digital Communications", second edition, Pearson Education, 2001.*
6. *Wayne Tomasi, "Advanced Electronic Communication Systems", 4th Edition PearsonEducation, 1998.*

COURSEARTICULATIONMATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**
CO2	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**
CO3	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**
CO4	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**
CO5	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**
25AEPC05	**3**	**2**	**-**	**2**	**2**	**1**	**-**	**-**	**2**	**-**	**1**	**2**	**1**	**1**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZMC001	Subject Title	RESEARCH METHODOLOGY AND IPR
Category	MC	L-T-P-C	2-0-0-2
Regulation	2025	Semester	III
Prerequisites	Basic research awareness and academic writing skills		

OBJECTIVES:

- To identify the problems and solutions for research in various areas
- To prepare literature survey and write thesis report
- To prepare research proposal in various agencies like DST, AICTE etc..,
- To understand the Intellectual property rights and patenting
- To understand the patent rights and its developments

RESEARCH PROBLEM AND SOLUTION (6 HOURS)

Meaning of research problem – Sources of research problem – Criteria Characteristics of a good research problem – Errors in selecting a research problem – Scope and objectives of research problem – Approaches of investigation of solutions for research problem – data collection – analysis – interpretation – Necessary instrumentations.

LITERATURE SURVEY AND WRITING (6 HOURS)

Effective literature studies approaches – Analysis – Plagiarism – Research ethics – Effective technical writing.

RESEARCH PROPOSAL (6 HOURS)

How to write report and Paper Developing a Research Proposal – Format of research proposal – a presentation and assessment by a review committee.

NATURE OF INTELLECTUAL PROPERTY (6 HOURS)

Patents – Designs – Trade and Copyright – Process of Patenting and Development: technological research – innovation – patenting – development – International Scenario: International cooperation on Intellectual Property – Procedure for grants of patents – Patenting under PCT.

PATENT RIGHTS AND NEW DEVELOPMENTS (6 HOURS)

Scope of Patent Rights – Licensing and transfer of technology – Patent information and databases – Geographical Indications – Administration of Patent System –IPR of Biological Systems – Computer Software etc – Traditional knowledge – Case Studies: IPR and IITs.

TOTAL :30 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand research problem identification, formulation, and approaches for solving research problems.	**L2**	PO3, PO8, PSO3
CO2	Apply research proposal writing techniques to develop structured research proposals.	**L3**	PO2, PO6, PO8, PSO2
CO3	Analyze literature, research ethics, plagiarism, and technical writing for effective documentation.	**L4**	PO4, PO9
CO4	Evaluate intellectual property rights, patents, and patenting procedures in research and innovation.	**L5**	PO10
CO5	Design and develop applications of IPR systems such as licensing, patent databases, and technology transfer strategies.	**L6**	PO11, PSO3

REFERENCES:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering
2. students"
3. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
4. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners" 2 nd Edition
5. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	-	-	2	-	-	-	-	2	-	-	-	-	-	3
CO2	-	-	-	2	-	-	-	-	2	-	-	-	-	-
CO3	-	2	-	-	-	3	-	1	-	-	-	-	2	-
CO4	-	-	-	-	-	-	-	-	-	2	-	-	-	-
CO5	-	-	-	-	-	-	-	-	-	-	1	-	-	3
25ZMC001	-	2	2	2	-	3	-	1	2	2	1	-	2	3

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPC06	Subject Title	ELECTRONIC SYSTEM DESIGN LABORATORY I
Category	PC	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I
Prerequisites	Electronic Circuits and Interfacing		

OBJECTIVES:

- To learn about the embedded hardware
- To become familiar with various interfacing techniques
- To learn about the implementation of functional modules in FPGA

LIST OF EXPERIMENTS USING ARM PROCESSOR:

1. Interfacing EEPROM using I2C.
2. Interfacing RF Transceiver using UART.
3. Interfacing DC motor & speed control using PWM.
4. Interfacing Temperature sensor using I2C.
5. Interfacing of Graphical LCD module.
6. Interfacing of RTC.
7. Interfacing of Stepper Motor.
8. Programming in RTOS environment
9. Data acquisition from a remote location and display using graphical LCD.
10. Implementation of Linear convolution using FPGA.
11. Implementation of FFT using FPGA.
12. Design of closed loop system using PROTEUS software.

TOTAL : 60 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the operation of embedded hardware peripherals and implement basic interfacing techniques using ARM processors.	L2	PO1, PO4, PO5, PO11
CO2	Apply communication protocols such as I²C and UART to interface embedded peripherals and develop embedded applications.	L3	PO1, PO2, PO5, PO7, PO8
CO3	Analyze embedded systems by integrating peripherals and validating system functionality in an RTOS environment.	L4	PO1, PO2, PO5, PO8, PO11
CO4	Evaluate the performance of real-time embedded systems through hardware interfacing, data acquisition, and simulation using PROTEUS.	L5	PO1, PO2, PO4, PO5, PO7, PO8, PO11
CO5	Design and implement DSP modules such as Linear Convolution and FFT using FPGA for real-time applications.	L6	PO1, PO2, PO7

COURSE ARTICULATION MATRIX:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	**3**	**-**	**-**	**1**	**2**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**-**	**-**
CO2	**2**	**2**	**-**	**-**	**3**	**-**	**1**	**1**	**-**	**-**	**-**	**-**	**2**	**-**
CO3	**2**	**3**	**-**	**-**	**3**	**-**	**-**	**2**	**-**	**-**	**1**	**3**	**2**	**-**
CO4	**2**	**3**	**-**	**1**	**3**	**-**	**3**	**2**	**-**	**-**	**3**	**3**	**1**	**-**
CO5	**2**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**3**	**3**	**2**
25AEPC06	**2**	**2**	**-**	**-**	**3**	**-**	**2**	**2**	**-**	**-**	**-**	**3**	**2**	**-**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

SEMESTER II

Subject Code	25AEPC07	Subject Title	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES
Category	PC	L-T-P-C	3-0-0-3
Regulation	2025	Semester	II
Prerequisites	Fundamentals of Artificial Intelligence		

OBJECTIVES:

- To classify various soft computing frame works.
- To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems.
- To learn mathematical background for optimized genetic programming.
- Be exposed to neuro-fuzzy hybrid systems and its applications.
- To understand the various evolutionary optimization techniques.

FUZZY LOGIC (9 HOURS)

Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.

ARTIFICIAL NEURAL NETWORKS (9 HOURS)

Supervised Learning: Introduction and how brain works, Neuron as a simple computing element,The perceptron, Back propagation networks: architecture, multilayer perceptron, back propagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network. Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self-Organizing Computational Maps: Kohonen Network.

GENETIC ALGORITHM (9 HOURS)

Genetic algorithm- Introduction - biological background - traditional optimization and search techniques -Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

NEURO-FUZZY MODELING (9 HOURS)

Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base StructureIdentification –Neuro-Fuzzy Control – the inverted pendulum system.

CONVENTIONAL OPTIMIZATION TECHNIQUES (9 HOURS)

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method,
external penalty function method

TOTAL:45PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of fuzzy sets, fuzzy logic, membership functions, and fuzzy inference systems for solving engineering problems.	**L2**	**PO1, PO2, PO3, PO10**
CO2	Apply artificial neural networks and genetic algorithms to develop intelligent systems for optimization and prediction.	**L3**	**PO1, PO2, PO3, PO10**
CO3	Analyze neural network learning algorithms, optimization methods, and evolutionary techniques for machine learning applications.	**L4**	**PO1, PO2, PO10**
CO4	Evaluate neuro-fuzzy models, clustering algorithms, and adaptive inference systems for classification and control applications.	**L5**	**PO1, PO2, PO3, PO5, PO6, PO10, PO11**
CO5	Design optimization models using conventional and evolutionary optimization techniques to solve real-world engineering problems.	**L6**	**PO1, PO2, PO3**

REFERENCES:

1. *J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI /Pearson Education2015*
2. *Timothy J.Ross, Fuzzy Logic with Engineering Applications, Wiley-Blackwell, FourthEdition 2016*
3. *George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Pearson Education2015*
4. *Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley &sons,inc,Fourth Edition, 2013*
5. *David E. Goldberg, Genetic Algorithms in Search, Optimization and MachineLearning, Addison wesley, 2009.*
6. *Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice HallInternational Inc, 2003.*
7. *James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications,and Programming Techniques, Pearson Edn., 2003.*
8. *Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.*

COURSEARTICULATIONMATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**2**	**2**	**-**
CO2	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**3**	**-**
CO3	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**-**	**3**	**2**	**-**
CO4	**2**	**3**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**2**	**2**	**3**	**2**	**-**
CO5	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**-**
25AEPC07	**2**	**3**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**2**	**2**	**3**	**2**	**-**

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation **BOS Approval**

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Subject Code	**25AEPC08**	**Subject Title**	**VLSI SYSTEM DESIGN**
Category	PC	**L-T-P-C**	3-0-0-3
Regulation	2025	**Semester**	II
Prerequisites	Verilog / VHDL Programming Basics		

OBJECTIVES:

- To study different types of programming technologies and logic devices.
- To gain knowledge about partitioning, floor planning and routing including circuit extraction of ASIC
- To know about different high performance algorithms and its applications in ASICs.

OVERVIEW OF ASIC AND PLD (9 HOURS)

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs –PLA –PAL. Gate Arrays – CPLDs and FPGAs

ASIC PHYSICAL DESIGN (9 HOURS)

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction -DRC.

LOGIC SYNTHESIS, SIMULATION ANDTESTING (9 HOURS)

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language -PLA tools -EDIF-CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

FIELD PROGRAMMABLE GATE ARRAYS (9 HOURS)

FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing – Register transfer(RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

SOC DESIGN (9 HOURS)

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera,SDRAM, High Speed Data standards.

TOTAL:45 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain ASIC design flow, programmable logic devices, and various programming technologies used in VLSI systems.	**L2**	**PO1, PO2, PO3, PO4, PO5, PO9, PO11**
CO2	Apply floor planning, partitioning, placement, and routing techniques in ASIC physical design.	**L3**	**PO1, PO2, PO3, PO4, PO5, PO9, PO11**
CO3	Analyze logic synthesis, simulation, and testing techniques using HDL-based	**L4**	**PO1, PO2, PO3, PO4,**

CO	Course Outcome	Bloom's Level	PO's Mapped
	design methodologies.		**PO5, PO9, PO11**
CO4	Analyze FPGA design flow, technology mapping, placement, routing, and logic optimization techniques.	**L4**	**PO1, PO2, PO3, PO4, PO5, PO9, PO11**
CO5	Design System-on-Chip (SoC) architectures and evaluate high-performance ASIC design issues and case studies.	**L5**	**PO1, PO2, PO3, PO4, PO5, PO9, PO11**

REFERENCES:

1. *M.J.S.Smith, "Application - Specific Integrated Circuits", Pearson, 2010.*
2. *Steve Kilts "Advanced FPGA Design", Wiley Inter-Science, 2007.*
3. *Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, "FPGA-Based Implementation of Signal Processing Systems", Wiley, 2008.*
4. *Michael J. Flynn, Wayne Luk,Computer System Design: System on chip,Wiley-Blackwell, First Edition, 2011.*
5. *Jose L. Ayala, Communication Architectures for Systems-on-Chip, CRC Press, First Edition,2011.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**3**	**2**	**2**	**2**	**3**	**-**	**-**	**-**	**2**	**-**	**1**	**2**	**2**	**-**
CO2	**3**	**2**	**2**	**2**	**2**	**-**	**-**	**-**	**2**	**-**	**1**	**2**	**2**	**-**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**2**	**-**	**1**	**3**	**3**	**-**
CO4	**3**	**3**	**2**	**2**	**3**	**-**	**-**	**-**	**2**	**-**	**1**	**3**	**3**	**-**
CO5	**3**	**2**	**2**	**2**	**2**	**-**	**-**	**-**	**2**	**-**	**1**	**2**	**2**	**-**
25AEPC08	**3**	**2**	**2**	**2**	**3**	**-**	**-**	**-**	**2**	**-**	**1**	**2**	**2**	**-**

1- Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Subject Code	25AEPC09	Subject Title	DIGITAL IMAGE PROCESSING
Category	PC	L-T-P-C	3-0-0-3
Regulation	2025	Semester	II
Prerequisites	Basic Programming (MATLAB / Python / C)		

OBJECTIVES:

- To introduce vision fundamentals and transforms for 2D signals
- To teach concepts for extracting images from their corresponding degraded version
- To introduce techniques for segregating and extracting objects in images
- To impart techniques for processing color images
- To teach efficient methods for storing and transmitting images

DIGITAL IMAGE FUNDAMENTALS (9 HOURS)

Elements of digital image processing systems, Digital Camera working principles, Elements of visualperception, Image sampling, Quantization, Dither, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

IMAGE ENHANCEMENT AND RESTORATION (9 HOURS)

Image Enhancement in the Spatial Domain - Basic Gray Level Transformations, Histogram Processing, Smoothing Spatial Filters, Sharpening Spatial Filters, Enhancement in the Frequency Domain- Smoothing Frequency-Domain Filters. Sharpening Frequency Domain Filters. Homomorphic Filtering, Image restoration - Model of the Image Degradation/Restoration Process. Noise Models. Restoration in the Presence of Noise Only-Spatial Filtering. Periodic Noise Reduction by Frequency Domain Filtering. Estimating the Degradation Function. Inverse Filtering. Minimum Mean Square Error (Wiener) Filtering.Constrained Least Squares Filtering. Geometric Transformations.

IMAGE SEGMENTATION AND MORPHOLOGY (9 HOURS)

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Morphological Image Processing - Basics, SE, Erosion, Dilation,Opening, Closing, Hit-or-Miss Transform, Boundary Detection, Hole filling, Connected components,convex hull, thinning, thickening, skeletons, pruning, Geodesic Dilation, Erosion, Reconstruction by dilation and erosion.

COLOR IMAGE PROCESSING (9 HOURS)

Color Fundamentals. Color Models. Pseudocolor Image Processing. Basics of Full-Color Image Processing. Color Transformations. Smoothing and Sharpening. Color Segmentation. Noise in Color Images. Color ImageCompression.

IMAGE COMPRESSION (9 HOURS)

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG, MPEG, Digital Image Watermarking.

TOTAL :45 PERIODS

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Apply image fundamentals, sampling, quantization, and transform techniques in digital image processing.	**L2**	**PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11**
CO2	Apply and analyze image enhancement and restoration techniques in spatial and frequency domains.	**L3**	**PO1, PO2, PO3, PO4, PO5, PO6, PO9, PO11**
CO3	Analyze and design image segmentation and morphological processing techniques for object extraction.	**L4**	**PO1, PO2, PO3, PO4, PO5, PO6, PO9, PO11**
CO4	Evaluate color image processing techniques including color models, transformations, and segmentation methods.	**L5**	**PO1, PO2, PO3, PO4, PO8, PO9, PO11**
CO5	Design and implement image compression algorithms using coding techniques and standards like JPEG and MPEG.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO11**

REFERENCES:

1. *Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education, Inc.,4th Edition, 2018*
2. *Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2015.*
3. *Rafael C. Gonzalez, Richard E. Woods, Steven Eddins, "Digital Image Processing usingMATLAB", Pearson*
4. *Education, Inc., 2nd Edition, 2010.*
5. *William K. Pratt, "Digital Image Processing", John Wiley, New York, 2002.*
6. *Scott E.Umbaugh,"Digital Image Enhancement Restoration and Compression",CRC press,4thEdition*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	1	1	-	3	2	-	2	2	1	-
CO2	2	2	3	2	2	1	-	2	1	-	1	2	2	-
CO3	3	2	3	2	1	1	-	2	1	-	2	2	2	1
CO4	3	3	2	2	-	-	-	-	2	-	2	3	2	-
CO5	3	2	2	2	2	2	1	3	2	-	2	2	2	2
25AEPC09	3	3	2	2	1	2	-	3	2	-	2	2	2	2

1-Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation **BOS Approval**

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	**25AEPC10**	**Subject Title**	**INTERNET OF THINGS**
Category	PC	**L-T-P-C**	3-0-0-3
Regulation	2025	**Semester**	II
Prerequisites	Basic understanding of **Microprocessors and Microcontrollers**		

OBJECTIVES:

- Understand the fundamentals of Internet of Things and its protocols.
- Explore and learn about Internet of Things with help of preparing projects designed for
- Raspberry Pi.
- Realize the concept of Internet of Things in the real-world scenario

IOT ARCHITECTURES AND MODELS (9 HOURS)

Introduction to IoT – IoT Architectures – Core IoT Functional Stack, Sensors and Actuators Layer, Communications Network Layer, Applications and Analytics Layer – IoT Data Management and Compute Stack, Fog Computing, Edge Computing, Cloud Computing – Sensors, Actuators and Smart Objects, Sensor networks.

CONNECTIVITY (9 HOURS)

Communications Criteria – Access Technologies – IP as IoT Network Layer – Business case – Optimization – Profiles and compliances – Application Protocols – Transport Layer – Application Transport Methods.

DATA ANALYTICS AND IoT SECURITY (9 HOURS)

Data Analytics for IoT – Machine Learning – Big Data Analytics Tools and Technology – Edge Streaming Analytics – Network Analytics, Applications. Security history, challenges, variations between IT and OT security – Risk Analysis Structures – Application in Operational Environment.

IoT IN INDUSTRY (9 HOURS)

Manufacturing – Utilities – Smart and Connected Cities – Transportation – Mining.

SYSTEM DEVELOPMENT (9 HOURS)

Design Methodology – Case study – Basic blocks of IoT device – Raspberry Pi – Board, Interfaces, Linux, Setting up, Programming – Arduino – Other IoT Devices.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain IoT architectures, functional stacks, sensors, actuators, and compute models such as edge, fog, and cloud computing.	**L2**	**PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO2, PSO3**
CO2	Analyze IoT connectivity technologies, network protocols, transport methods, and application layer communications.	**L3**	**PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO2, PSO3**
CO3	Analyze IoT data analytics techniques and evaluate security challenges in IoT systems.	**L4**	**PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO2, PSO3**

CO	Course Outcome	Bloom's Level	PO's Mapped
CO4	Evaluate IoT applications in industrial domains such as smart cities, transportation, utilities, and mining.	L5	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO2, PSO3
CO5	Design and develop IoT applications using platforms like Raspberry Pi and Arduino for real-world systems.	L6	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO2, PSO3

REFERENCES:

1. *David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, "IoT*
2. *Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things", CiscoPress, 2017*
3. *Arshdeep Bahga, Vijay Madisetti, "Internet of Things – A hands-on approach",Universities Press,*
4. *2015.*
5. *Jan Holler, Vlasios Tsiatsis , Catherine Mulligan, Stamatis , Karnouskos, StefanAvesand. David Boyle,*
6. *"From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", 2nd Edition, Elsevier, 2018.*
7. *Wiley Editorial,"Internet of Things,An Indian Adaptation: :Comcepts and Applications", Wiley, 2021.*
8. *F. John Dian," Fundamentals of Internet of Things: For Students and Professionals",Wiley, 2022.*
9. *Raj Kamal, "Internet of Things Architecture and Design Principles", 2nd Edition, TataMcGraw Hill,*
10. *2022.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	2	2	2	2	2	-	-	-	2	-	-	3	3	1
CO2	3	2	2	2	2	-	-	-	2	-	-	3	3	1
CO3	3	2	2	2	2	-	-	-	2	-	-	3	3	1
CO4	2	3	2	3	2	-	-	-	2	-	-	3	3	1
CO5	3	3	2	3	2	-	-	-	2	-	-	3	3	1
25AEPC10	3	2	2	2	2	-	-	-	2	-	-	3	3	1

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
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M.E. APPLIED ELECTRONICS

Subject Code	**25AEPC11**	**Subject Title**	**ELECTRONIC SYSTEM DESIGN LABORATORY II**
Category	PC	**L-T-P-C**	0-0-4-2
Regulation	2025	**Semester**	II
Prerequisites	FPGA Architecture fundamentals		

OBJECTIVES:

- To Learn Hardware Descriptive Language(Verilog/VHDL)
- To Implementation of FIR and IIR Filters
- To Familiarize with the design of various sequential and combinational digital circuits

LIST OF EXPERIMENTS

1. Edge detection using python program
2. Image thinning using Matlab program
3. Synthesize and Implement combinational and sequential circuits in verilog/VHDL
4. Synthesize and Implement MAC unit and GCD unit in verilog/VHDL.
5. Design and Implement FIR and IIR weiner filters for smoothing and prediction
6. write a program to implement artificial neural network with/without back propagation
7. EMI measurements and control test for DUT using Anechoic chamber.
8. conducted Emission test using LISN
9. Range finder using Arduino
10. Weather monitoring system using arduino
11. Smart lighting home automation
12. Home security or interactive home detection

TOTAL :60 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain fundamental concepts and basic principles of the course domain.	L2	PO1, PO2, PO4, PO5, PO9
CO2	Apply learned concepts and methods to solve standard problems.	L3	PO1, PO2, PO3, PO4, PO5
CO3	Analyze systems, models, and relationships among components.	L4	PO1, PO2, PO3, PO4, PO5, PO9
CO4	Evaluate techniques, methods, and solutions based on given criteria.	L5	PO1, PO2, PO3, PO4, PO5, PO9
CO5	Design and develop new systems, models, or solutions for real-world applications.	L6	PO1, PO2, PO3, PO4, PO5, PO9

COURSE ARTICULATION MATRIX:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	-	-	3	-	2	2	1	2
CO2	2	2	2	2	2	3	-	-	3	-	2	2	2	2
CO3	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO4	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO5	2	2	2	3	3	3	-	-	3	-	2	3	3	2
25AEPC11	2	2	2	3	3	3	-	-	3	-	2	3	3	2

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Subject Code	25AEEE12	Subject Title	TERM PAPER WRITING AND SEMINAR
Category	EEC	L-T-P-C	0-0-2-1
Regulation	2025	Semester	II
Prerequisites	Ability to search and read technical papers, journals, and articles		

COURSE OBJECTIVES:

- To identify the specific research topic.
- To analyze the research findings in conventional papers.
- To organize the modules and write a technical paper.

The procedure for writing a term paper may consist of the following steps:

- Choosing a subject
- Finding sources of materials
- Collecting the notes
- Outlining the paper
- Writing the first draft
- Editing & preparing the final paper

Choosing a Subject

The subject chosen should not be too general and relevant to the curriculum.

Finding Sources of materials

- The material sources should be not more than 10 years old unless the nature of the paper is such that it involves examining older writings from a historical point of view.
- Begin by making a list of subject-headings under which you might expect the subject to be listed.
- The sources could be conferences, symposia or workshops, journals etc.

Collecting the notes

Skim through sources, locating the useful material, then make good notes of it, including quotes and information for footnotes.

- Get facts, not just opinions. Compare the facts with author's conclusion.
- In research studies, notice the methods and procedures, results & conclusions.
- Check cross references.

Outlining the paper

- Review notes to find main sub-divisions of the subject.
- Sort the collected material again under each main division to find sub-sections for outline so that it begins to look more coherent and takes on a definite structure. If it does not, try going back and sorting again for main divisions, to see if another general Pattern is possible

Writing the first draft

Write the paper around the outline, being sure that you indicate in the first part of the paper what its purpose is.
You may follow the following:
a) statement of purpose
b) main body of the paper
c) statement of summary and conclusion
Avoid short, bumpy sentences and long straggling sentences with more than one main idea.

Editing & Preparing the final Paper

d) Before writing a term paper, you should ensure you have a question which you attempt to answer in your paper. This question should be kept in mind throughout the paper. Include only information/ details/ analyses of relevance to the question at hand. Sometimes, the relevance of a particular section may be clear to you but not to your readers. To avoid this, ensure you briefly explain the relevance of every section.

e) Read the paper to ensure that the language is not awkward, and that it "flows" properly.

f) Check for proper spelling, phrasing and sentence construction.

g) Check for proper form on footnotes, quotes, and punctuation.

h) Check to see that quotations serve one of the following purposes:

i) Check for proper form on tables and graphs. Be certain that any table or graph is self- explanatory.

Final report Submission

It should have up to 2000 – 2500 words excluding Preface, copy right index etc. Copies Required: 2 copies: Plastic Spiral bound. One Soft copy

Seminar:up to 2500 – 3000 words text excluding Preface, Certificate Index etc. Copies Required: 1 copy: Plastic Spiral bound One Soft copy with all figs and ref.

Conduct & Progress Monitoring of Term Paper

a) The students will regularly report to their faculty guide for their weekly progress as per the prescribe format of Weekly Progress Report (WPR).

b) Faculty guide will mark the status of Weekly Progress Report (WPR) received and quality of work done. Faculty guide will also give feedback to students concerning the progress.

c) The student will also maintain daily diary of the work done which need to be submitted to the faculty guide.

d) The student will maintain the record of interaction and feedback by Faculty Guide as per the format attached.

Technical Seminar

During the seminar session each student is expected to prepare and present a topic on engineering / technology, for duration of about 8 to 10 minutes. In a session of three periods Per week, students are expected to present the seminar. A faculty guide is to be allotted and he / she will guide and monitor the progress of the student and maintain attendance also. Students are encouraged to use various teaching aids such as overhead projectors, power point presentation and demonstrative models. This will enable them to gain confidence in facing the placement interviews.

Conduct & Progress Monitoring of Technical Seminar

- To encourage the students to study advanced engineering developments
- To prepare and present technical reports.
- To encourage the students to use various teaching aids such as overhead projectors,power point presentation and demonstrative models.

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Analyze technical literature and prepare a structured literature survey.	L4	PO1, PO2, PO4, PO9, PO10
CO2	Prepare and present a technical seminar on a selected engineering topic.	L3	PO9, PO10, PO11
CO3	Discuss and respond to queries related to the chosen technical topic.	L2	PO9, PO10, PO11

Course Designed By

Name & Designation **BOS Approval**

Date:

SEMESTER III

Subject Code	25AEEE15	Subject Title	DISSERTATION - I
Category	EEC	L-T-P-C	0-0-12-6
Regulation	2025	Semester	III
Prerequisites	Fundamentals of data analysis and problem-solving techniques		

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Usage of mathematical, computational and natural sciences gained by study, experience and practice with judgment
- Develop effective use of matter, energy and information to the benefit of mankind.
  Plan, execute, manage and document a project

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Identify research-intensive and feasible problems considering societal and industrial needs.	L3	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1
CO2	Perform an exhaustive literature survey on the identified research problem.	L4	PO1, PO2, PO4, PO6, PO9, PO10, PO11, PSO1, PSO3
CO3	Use design and simulation tools to implement and validate methods or algorithms from literature.	L5	PO1, PO2, PO4, PO6, PO7, PO9, PO10, PO11, PSO1, PSO3
CO4	Develop and deliver effective technical presentations for research communication.	L2	PO4, PO9, PO10, PO11, PSO1
CO5	Write clear, concise, and publication-quality technical documents for research dissemination.	L6	PO1, PO2, PO4, PO6, PO8, PO9, PO10, PO11, PSO2, PSO3

COURSE ARTICULATION MATRIX:														
	PROGRAM OUTCOMES											PROGRAM SPECIFIC OUTCOMES		
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	3	1	3	2	3	3	2	3	3	1	1
CO2	3	2	1	3	1	3	2	1	3	2	3	3	1	3
CO3	2	2	1	3	1	3	3	1	3	2	3	3	1	3
CO4	2	2	1	2	2	2	3	1	2	2	1	2	3	3
CO5	3	2	2	2	2	2	3	3	2	2	1	2	2	3
(1- Low, 2- Moderate, 3-High)														

Course Designed By

Name & Designation

BOS Approval

Date:

SEMESTER – IV

Subject Code	**25AEEE16**	**Subject Title**	**DISSERTATION - II**
Category	EEC	**L-T-P-C**	0-0-24-12
Regulation	2025	**Semester**	IV
Prerequisites	Data analysis, validation, and performance evaluation techniques		

COURSE OBJECTIVES:

Upon completion of this course, the students will be familiar with:

- Usage of mathematical, computational and natural sciences gained by study, experience and practice with judgment to develop effective use of matter, energy and information to the benefit of mankind.
- Plan, execute, manage and document a project
- Construct logical and physical models to demonstrate the skills at assimilating, synthesizing and critically appraising all materials relevant to the project.

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the theoretical and practical aspects of the identified research problem and implementation approach.	**L2**	PO1, PO2, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO3
CO2	Apply advanced tools or develop new tools for implementing the proposed research methodology.	**L3**	PO1, PO2, PO4, PO5, PO6, PO7, PO8, PO9, PO11, PSO1, PSO3
CO3	Analyze and compare the performance of proposed methods with existing approaches to validate results.	**L4**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO3
CO4	Evaluate the correctness and effectiveness of proposed solutions through exhaustive testing and validation.	**L5**	PO1, PO2, PO4, PO5, PO6, PO7, PO8, PO9, PO11, PSO1, PSO3
CO5	Create and present high-quality technical documentation suitable for journal or conference publication.	**L6**	PO1, PO2, PO4, PO6, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3

COURSE ARTICULATION MATRIX:														
	PROGRAM OUTCOMES											PROGRAM SPECIFIC OUTCOMES		
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1	3	1	3	2	3	3	2	3	3	1	2
CO2	3	2	1	3	2	3	2	3	3	1	3	1	1	2
CO3	3	3	1	3	2	3	3	3	3	2	3	1	1	2
CO4	3	3	2	2	2	3	3	3	2	2	3	2	3	3
CO5	3	3	2	2	2	3	3	3	2	2	3	2	2	2
(1- Low, 2- Moderate, 3-High)														

Course Designed By

Name & Designation

BOS Approval

Date:

PROFESSIONAL ELECTIVES (PE)

Subject Code	25AEPE01	Subject Title	DIGITAL CONTROL ENGINEERING
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**Control Systems Engineering** (Time response, frequency response, stability concepts)		

OBJECTIVES:

- To studythe principles of PI,PD,PID controllers.
- To analyse time and frequency response discrete time control system.
- To familiarize and practice digital control algorithms
- To implement PID control algorithms using microprocessors, microcontrollers.

CONTROLLERS IN FEEDBACK SYSTEMS (9 HOURS)

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS (9 HOURS)

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model ofsample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction

MODELING OF SAMPLED DATACONTROLSYSTEM (9 HOURS)

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems,Jury's stability test,state spaced escription,first companion,second companion,Jordan Canonical models, discrete state variable models (elementary principles only).

DESIGN OF DIGITAL CONTROL ALGORITHMS (9 HOURS)

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

PRACTICAL ASPECTS OF DIGITALCONTROLALGORITHMS (9 HOURS)

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability to

CO No.	Course Outcome	Bloom's Level	PO Mapping
CO1	Describe continuous-time and discrete-time control systems and controller structures (PI, PD, PID).	L2	PO1, PO2, PO9, PO12

CO2	Explain sampling process, quantization, reconstruction, and digital signal processing concepts in control systems.	L3	PO1, PO2, PO3, PO5
CO3	Analyze discrete-time control systems using Z-transform, pulse transfer function, and stability methods.	L4	PO1, PO2, PO4, PO5, PO12
CO4	Design digital controllers (especially PID) in the Z-domain using frequency and time-domain specifications.	L5	PO1, PO2, PO3, PO4, PO5, PO12
CO5	Implement digital control algorithms using microcontrollers/DSP for real-time applications.	L6	PO2, PO3, PO5, PO9, PO10, PSO1, PSO3

REFERENCES:

1. *loan D, Landau and GianLuca Zito "Digital Control Systems _ Design, Identification and Implementation", 2005.*

2. *M.Sami Fadali, Antonio Visioli "Digital Control Engineering _ Analysis and Design "Second edition 2013*
3. *M.Gopal,"DigitalControlandStaticVariableMethods",TataMcGrawHill,NewDelhi,1997.*
4. *JohnJ.D'Azzo,"ConstantiveHoupios,"LinearControlSystemAnalysisandDesign",Mc Graw Hill,1995.*
5. *KennethJ.Ayala,"The8051Microcontroller-Architecture,Programming andApplications",Penram International,2nd Edition,1996.*
6. *loan D, Landau and GianLuca Zito "Digital Control Systems - New edition, 2020.*
7. *Rolf Isermann "Digital Control Systems" Volume 1, Fundamentals, Deterministic Control2nd Revised Edition, 1989.*
8. *William S .Levine, The Control Handbook, Second Edition "Control System Fundamentals"CRC Press, Taylor and Francis Group.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	2	2	-	-	-	-	-	-	1	1	-	3	2	1
CO2	1	2	1	1	2	2	-	-	1	1	-	3	2	1
CO3	3	2	2	1	1	3	1	-	1	-	-	3	2	1
CO4	1	2	2	3	1	2	2	1	1	1	1	3	2	2
CO5	2	2	2	2	2	3	1	2	2	1	1	3	2	3
25AEPE01	3	2	2	3	2	3	2	2	2	1	1	3	2	3

1- Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE02	Subject Title	COMPUTER ARCHITECTURE
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**Control Systems Engineering** (Time response, frequency response, stability concepts)		

OBJECTIVES:

- To understand the difference between pipeline and parallel processing concepts
- To study various types of processor architectures and the importance of scalable architectures
- To study Memory Optimization and Technique.

COMPUTER DESIGN AND PERFORMANCEMEASURES (9 HOURS)

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi- vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures

PARALLEL PROCESSING, PIPELINING AND ILP (9 HOURS)

Instruction Level Parallelism - Concepts and Challenges - Pipelining processors –The MIPS R4000 Pipeline-Thread level parallelism-Overcoming Data Hazards with Dynamic Scheduling – Exploiting ILP using Multiple Issues of static and Dynamic scheduling-Studies of the limitations of ILP.

MEMORY HIERARCHY (9 HOURS)

Design Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Replacement Policies and Virtual Memory - Design of Memory Hierarchies.

MULTI PROCESSORS (9 HOURS)

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

MULTI-CORE ARCHITECTURES (9 HOURS)

Homogeneous and Heterogeneous Multicore architecture- Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand computer design fundamentals, scalable architectures, SIMD/MIMD systems, and performance measures	L2	PO1, PO2, PO3, PO10, PO12
CO2	Apply concepts of pipelining, ILP, and parallel processing with hazard mitigation techniques	L3	PO1, PO2, PO3, PO10, PO12
CO3	Analyze memory hierarchy design, cache optimization, and virtual memory systems	L4	PO1, PO2, PO6, PO9, PO11, PO12
CO4	Evaluate multiprocessor systems including cache coherence, synchronization, and memory consistency models	L5	PO1, PO2, PO3, PO6, PO7, PO10, PO12
CO5	Design and develop multicore architectures and compare modern processor architectures	L6	PO1, PO2, PO3, PO10, PO12

REFERENCES:

1. *Kai Hwang, Naresh Jotwani "Advanced Computer Architecture" parallelism, scalableprogrammability ,2016*
2. *Sajjan G.Shiva "Advanced computer Architecture',2018*
3. *John L. Hennessey and David A. Patterson, "Computer Architecture – A quantitative approach", Morgan Kaufmann / Elsevier, 4th. edition, 2007.*
4. *Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: DesignMethodologies and Tools", Springer, 2012.*
5. *Darryl Gove- Multicore Application programming: For Windows , Linux, and Oraclesolaris,pearson,2011.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	3	3	2	-	-	-	-	-	-	3	-	2	2	-
CO2	2	3	1	1	-	-	-	-	-	2	-	2	1	-
CO3	2	2	1	-	-	2	-	-	-	1	1	2	2	-
CO4	2	3	2	1	-	2	1	-	-	2	-	2	2	-
CO5	2	2	2	-	-	-	-	-	-	2	-	2	1	-
25AEPE02	2	3	2	-	-	2	1	-	-	2	1	2	2	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE03	Subject Title	DIGITAL VLSI DESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	II
Prerequisites	Semiconductor Physics and Devices		

OBJECTIVES:

- To understand the principles of MOS transistor and CMOS inverter.
- To study the various latches and registers, layout and stick diagram of digital circuits.
- To gain knowledge about different building blocks and architecture.

MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER (9 HOURS)

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

COMBINATIONAL LOGIC CIRCUITS (9 HOURS)

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore‟s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

SEQUENTIAL LOGIC CIRCUITS (9 HOURS)

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier-based Registers, Nonbistable Sequential Circuits.

ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES (9 HOURS)

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

INTERCONNECT AND CLOCKING STRATEGIES (9 HOURS)

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL:45 PERIODS

Upon completion the course, the students will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the principles, characteristics, and operation of MOS transistors and CMOS inverter circuits for digital system design.	**L2**	**PO1, PO2, PO3, PO9, PO11, PSO1, PSO2**
CO2	Apply CMOS design techniques, stick diagrams, and layout methods for implementing combinational logic circuits.	**L3**	**PO1, PO2, PO3, PO9, PO11, PSO1, PSO2, PSO3**
CO3	Analyze sequential logic circuits including latches, registers, timing issues, and pipeline structures.	**L4**	**PO1, PO2, PO3, PO9, PO11, PSO1, PSO2, PSO3**
CO4	Evaluate different arithmetic building blocks, memory architectures, and design trade-offs in CMOS VLSI systems.	**L5**	**PO1, PO2, PO3, PO9, PO11, PSO1, PSO2, PSO3**
CO5	Design and optimize CMOS VLSI systems by analyzing interconnect effects, clocking strategies, power, speed, and area constraints.	**L6**	**PO1, PO2, PO3, PO9, PO11, PSO1, PSO2, PSO3**

REFERENCES:

1. *Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.*
2. *N.Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addison Wesley, 1993.*
3. *Jacob Baker, "CMOS: Circuit Design, Layout, and Simulation", Third Edition Wiley IEEE Press 2010.*
4. *Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.*
5. *M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO 1	PSO2	PSO3
CO1	3	3	2	_	_	_	_	_	2	_	2	3	3	_
CO2	3	3	2	_	_	_	_	_	2	_	2	2	2	_
CO3	3	2	2	_	_	_	_	_	2	_	2	2	2	_
CO4	3	3	2	_	_	_	_	_	2	_	2	3	3	_
CO5	3	2	2	_	_	_	_	_	2	_	2	2	2	_
20AEPE03	3	3	2	_	_	_	_	_	2	_	2	2	2	_

1-Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE04	Subject Title	EMI AND EMC IN SYSTEM DESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Basic knowledge of **electromagnetism, electronic circuits, network theory, and PCB fundamentals** to understand EMI/EMC concepts		

OBJECTIVES:

- To understand the concepts related to Electromagnetic interference in PCBs.
- To provide solutions for minimizing EMI in PCBs .
- To learn various EMI coupling principles.
- To indulge knowledge on EMI control techniques and design procedures to make EMI compatible PCBs
- To learn electromagnetic compatibility issues with regard to the design of PCBS
- To learn, EMI standards and measurements in the design of PCBs

EMI/EMC CONCEPTS (9 HOURS)

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards**.**

EMI COUPLING PRINCIPLES (9 HOURS)

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling,cross talk ; Field to cablecoupling ; Power mains and Power supply coupling.

EMI CONTROL TECHNIQUES (9 HOURS)

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing,Signal control.

EMC DESIGN OF PCBS (9 HOURS)

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

EMI MEASUREMENTS AND STANDARDS (9 HOURS)

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx/Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer;Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability to

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand EMI/EMC concepts, sources, effects, and EMI/EMC parameters in electronic systems	L2	PO1, PO2, PO3, PO4, PO9, PO10, PO11
CO2	Apply EMI coupling mechanisms including conducted, radiated, and transient coupling effects	L3	PO1, PO2, PO3, PO5, PO10, PO11, PSO3
CO3	Analyze EMI control techniques such as shielding, grounding, filtering, and isolation methods	L4	PO1, PO2, PO3, PO4, PO5, PO12, PSO1
CO4	Evaluate EMI/EMC issues in PCB design and propose design improvements for compliance	L5	PO1, PO2, PO3, PO4, PO5, PO6, PO12, PSO1, PSO3
CO5	Design EMI measurement setups and interpret international EMC standards and testing methods	L6	PO1, PO2, PO3, PO4, PO5, PO6, PO10, PO11, PO12, PSO2

REFERENCES:

1. *Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press,SecondEdition, Indian Edition, 2013.*
2. *Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008*
3. *Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010*
4. *Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc,Newyork,2009.*
5. *Electromagnetic Compatibility by Norman Violette ,Published by Springer, 2013.*
6. *Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.*
7. *Clayton Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience,2006.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO 3
CO1	2	1	3	1	1	1	1	1	2	1	1	1	1	1
CO2	2	1	1	1	1	1	1	1	1	1	2	1	1	2
CO3	3	2	3	1	1	1	1	1	1	1	1	2	2	1
CO4	2	1	3	3	2	3	1	1	1	1	1	2	2	2
CO5	3	2	1	3	3	3	2	2	2	1	1	1	1	1
25AEPE04	3	2	3	3	3	3	2	2	2	1	2	2	2	2

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE05	Subject Title	CAD FOR VLSI
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Digital electronics, switching theory, computer organization, and basic programming concepts		

OBJECTIVES:

- To introduce the VLSI design methodologies and design methods.
- To study algorithms for partitioning and placement.
- To study algorithms for floor planning and routing.
- To study algorithms for modelling, simulation and synthesis.

INTRODUCTION TO VLSI DESIGN FLOW (9 HOURS)

Introduction to VLSI Design methodologies and software tools , Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

LAYOUT, PLACEMENT AND PARTITIONING (9 HOURS)

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

FLOOR PLANNING AND ROUTING (9 HOURS)

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Arearouting, Channel routing, Global routing, Algorithms for global routing

SIMULATION AND LOGIC SYNTHESIS (9 HOURS)

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation,Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

HIGH LEVEL SYNTHESIS (9 HOURS)

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand VLSI design methodologies, design flow, and basic design automation tools	L2	PO1, PO2, PO3, PO10, PO12
CO2	Apply placement and partitioning algorithms for circuit layout optimization	L3	PO1, PO2, PO3, PO4, PO5, PO12
CO3	Analyze floor planning and routing techniques for VLSI circuit design	L4	PO1, PO2, PO3, PO4, PO5, PO12
CO4	Evaluate simulation and logic synthesis methods for digital circuits	L5	PO1, PO2, PO3, PO4, PO5, PO10, PO12
CO5	Design high-level synthesis solutions using scheduling, allocation, and assignment techniques	L6	PO1, PO2, PO3, PO4, PO5, PO12

REFERENCES:

1. *Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India,2017.*
2. *Naveed a. Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition,Springer,2017.*
3. *Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu,VLSI Physical Design: From GraphPartitioning to Timing Closure, Springer, 2011.*
4. *H. Yosuff and S.M. Sait, VLSI Physical Design Automation – Theory and Practice,Cambridge India, 2010.*
5. *Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer India, 2011.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	-	-	-	2	-	1	3	3	-
CO2	3	3	2	3	2	-	-	-	2	-	1	2	2	-
CO3	3	3	2	3	2	-	-	-	2	-	1	2	2	-
CO4	3	2	2	2	3	-	-	-	2	-	1	3	3	-
CO5	3	2	2	2	2	-	-	-	2	-	1	2	2	-
25AEPE05	3	3	2	2	3	-	-	-	2	-	1	2	2	-

1- Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE06	Subject Title	NANO ELECTRONICS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**semiconductor physics, electronic devices, solid-state electronics, and material science** to understand nanoelectronic devices, sensors, and photonic materials.		

OBJECTIVES:

- To learn and understand basic concepts of Nano electronics.
- To know about electronic and photonic materials.
- To understand how the transistor as Nano device.

SEMICONDUCTOR NANO DEVICES (9 HOURS)

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single- Electron Transistors; Nano robotics and Nano manipulation; Mechanical Molecular Nano devices; Nano computers:Optical Fibers for Nano devices; Photochemical Molecular Devices; DNA-Based Nano devices; Gas-BasedNano devices.

ELECTRONIC AND PHOTONIC MOLECULARMATERIALS (9 HOURS)

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers: - Quantum cascade lasers-Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers: - White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

THERMAL SENSORS (9 HOURS)

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors -Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

GAS SENSOR MATERIALS (9 HOURS)

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

BIOSENSORS (9 HOURS)

Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the principles and operation of semiconductor nano devices and nanoelectronic systems.	L2	PO1, PO10, PSO1, PSO2
CO2	Apply concepts of nano fabrication and electronic/photonic materials for nano device design.	L3	PO1, PO10, PSO1, PSO2
CO3	Analyze the design and operation of thermal, electromagnetic, mechanical, chemical, and optical sensors.	L4	PO1, PO2, PO6, PO10, PO11, PSO1, PSO2
CO4	Evaluate gas sensor materials and semiconductor-based gas sensing	L5	PO1, PO2, PO5, PO6, PO10,

CO	Course Outcome	Bloom's Level	PO's Mapped
	techniques for specific applications.		PSO1, PSO2
CO5	Design biosensor-based nano systems for biomedical and photonic applications.	L6	PO1, PO4, PO5, PO10, PSO1, PSO2

REFERENCES:

1. *M. Wilson, K. Kannangara, G Smith, M. Simmons, B. Raguse," Nanotechnology: Basicscience and Emerging technologies", Overseas Press India Pvt Ltd, New Delhi, First Edition, 2005.*
2. *G.W. Hanson," Fundamentals of Nano electronics", Pearson, 2009.*
3. *Akifumi Kawamura, Takashi Miyata, in "Biomaterials Nanoarchitectonics", 2016.*
4. *Brajesh Kumar Kaushik , "Nano Electronics-Devices,Circuits and Systems" 2018.*
5. *W. Ranier, "Nano Electronics and Information Technology", Wiley, -2008.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	-	-	-	-	-	-	-	3	-	3	2	-
CO2	3	-	-	-	-	-	-	-	-	2	-	3	2	-
CO3	2	2	-	-	-	2	-	-	-	1	1	3	2	-
CO4	2	2	-	-	2	2	-	-	-	2	-	3	2	-
CO5	2	1	-	3	1	-	-	-	-	2	-	3	2	-
25AEPE06	3	2	-	2	1	2	-	-	-	2	1	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE07	Subject Title	SENSORS AND SIGNAL CONDITIONING
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	sensor principles, signal conditioning, and actuator applications.		

OBJECTIVES:

- To know the static and dynamic characteristics of measurement systems.
- To studyabout the various types of sensors viz. Resistive, Reactive and Self- generating sensors.
- To know the different types of digital and semiconductor device sensors.

SENSOR CHARACTERISTICS (9 HOURS)

General concepts of sensors and its terminology, sensor classification, general input-output configuration, performance of static characteristics measurement systems, accuracy, precision, sensitivity, systematic errors , random errors, dynamic characteristics of measurement systems: zero- order, first-order, and second-order measurement systems and response.

RESISTIVE AND REACTIVE SENSORS (9 HOURS)

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors,light- dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & applicationtothe LVDT.

SELF-GENERATING SENSORS (9 HOURS)

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors:chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

ACTUATORS DRIVE CHARACTERISTICS ANDAPPLICATIONS (9 HOURS)

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motorcontrol, 4to 20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to- digital and digital-to-resolver converters.

DIGITAL SENSORS AND SEMICONDUCTORDEVICE SENSORS (9 HOURS)

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wirestrain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors, ultrasonic sensors, fiber-optic sensors.

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the characteristics and performance parameters of sensors and measurement systems.	L2	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11, PSO1, PSO2, PSO3
CO2	Apply the principles of resistive and reactive sensors with appropriate signal conditioning techniques.	L3	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11, PSO1, PSO2, PSO3
CO3	Analyze the operation and signal conditioning of self-generating sensors for engineering applications.	L4	PO1, PO2, PO3, PO4, PO5, PO6, PO9, PO11, PSO1, PSO2, PSO3
CO4	Evaluate the characteristics and applications of actuators and their drive systems.	L5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11, PSO1, PSO3
CO5	Design sensor-based measurement systems using digital and semiconductor device sensors for practical applications.	L6	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11, PSO1, PSO3

REFERENCES:

1. *Ramon Pallás - Areny, John G. webster,"Sensors and Signal Conditioning",second edition,2012.*
2. *Apurbar Das," Signal Conditioning", Springer-Verlag Berlin and Heidelberg GmbH&Co.KG, 2014.*
3. *Kevin James," PC Interfacing and Data acquisition", Elsevier, 2011.*
4. *Graham Brooker," Introduction to Sensors for ranging and imaging", Yesdee, 2009.*
5. *Ian Sinclair, "Sensors and Transducers", Elsevier, Third Edition, 2011..*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	2	2	-	1	3	-	2	2	1	2
CO2	1	2	2	2	2	3	-	1	3	-	2	2	2	2
CO3	2	2	2	3	3	3	-	-	3	-	2	3	3	2
CO4	2	2	2	3	3	3	-	1	3	-	2	3	-	2
CO5	2	2	2	3	3	3	-	1	3	-	2	3	-	2
25AEPE07	2	2	2	3	3	3	-	1	3	-	2	3	-	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE08	Subject Title	MEMS AND NEMS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**semiconductor devices, electronic circuits, material science, microfabrication concepts, and engineering mechanics** to understand MEMS/NEMS devices, fabrication technologies, sensors, and actuators.		

OBJECTIVES:

- To introduce the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.

INTRODUCTION TO MEMS AND NEMS (9 HOURS)

Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications Devices and structures. Materials for MEMS and NEMS: Silicon, silicon compounds, polymers, metals.

MEMS FABRICATION TECHNOLOGIES (9 HOURS)

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Evaporation, Electroplating; Etching techniques, Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology.

MICRO SENSORS (9 HOURS)

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

MICRO ACTUATORS (9 HOURS)

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsionbar, Comb drive actuators),Case study: RF switch.

NANO SYSTEMS AND QUANTUM MECHANICS (9 HOURS)

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization.

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the fundamentals, materials, applications, and operating principles of MEMS and NEMS devices.	**L2**	PO1, PO5, PO6, PO8, PO9, PO10, PSO1, PSO2
CO2	Apply MEMS fabrication technologies to design micro devices and microsystems.	**L3**	PO1, PO2, PO3, PO5, PO7, PSO1, PSO2
CO3	Analyze the design and operating principles of MEMS-based microsensors for engineering applications.	**L4**	PO1, PO2, PO4, PO6, PO11, PSO1, PSO2
CO4	Evaluate the performance and design approaches of micro actuators using different actuation mechanisms.	**L5**	PO1, PO2, PO3, PO7, PO8, PO10, PSO1, PSO2

CO	Course Outcome	Bloom's Level	PO's Mapped
CO5	Design MEMS/NEMS-based micro and nano systems by integrating quantum mechanics and nanotechnology concepts for advanced applications.	L6	PO2, PO3, PO5, PO6, PO8, PO9, PO11, PSO1, PSO2

REFERENCES:

1. *Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.*
2. *Sergey Edward Lyshevski "MENS and NEMS systems ,Devices and structures,2018*
3. *Edward B.Magrab "Vibration of Elastic systems with applications to MENS and NEMS,SpringerNetherlands,2012*
4. *Zhuoqing Yang, "Advanced MENS/ NEMS Fabrication and Sensors ,springer International*
5. *publishing,2021.*
6. *Tai-Ran Hsu, "MEMS and Microsystems Design ,Manufacture ,and Nanoscale Engineering",Wiley,2020*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	-	-	-	2	2	-	3	2	3	-	3	2	-
CO2	2	2	2	-	2	-	3	-	-	-	-	3	2	-
CO3	2	3	-	2	-	2	-	-	-	-	3	3	2	-
CO4	2	3	2	-	-	-	2	2	-	2	-	3	2	-
CO5	-	2	2	-	3	2	-	2	2	-	2	3	2	-
25AEPE08	-	-	-	2	3	3	-	-	2	-	-	3	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE09	Subject Title	DSP INTEGRATED CIRCUITS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**semiconductor devices, electronic circuits, material science, microfabrication concepts, and engineering mechanics** to understand MEMS/NEMS devices, fabrication technologies, sensors, and actuators.		

OBJECTIVES:

- To impart knowledge on fundamental signal processing algorithms and systems.
- To expose digital filter concepts, structures and hardware issues
- To understand the various modules used in general purpose digital signal processors.
- To introduce various implementation strategies for signal processing algorithms
- To gain knowledge for tuning signal processing algorithms for VLSI.

INTRODUCTION TO DSP INTEGRATEDCIRCUITS (9 HOURS)

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

DIGITAL FILTERS AND FINITE WORD LENGTHEFFECTS (9 HOURS)

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

DSP ARCHITECTURES (9 HOURS)

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

SYNTHESIS OF DSP ARCHITECTURES (9 HOURS)

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements –clocking of synchronous systems, Asynchronous systems -FSM

ARITHMETIC UNIT AND PROCESSING ELEMENTS (9 HOURS)

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the fundamentals of digital signal processing algorithms, systems, and integrated circuit design.	**L2**	PO1, PO2, PO3, PO10, PSO1, PSO2
CO2	Apply digital filter design techniques and analyze finite word length effects in DSP systems.	**L3**	PO1, PO2, PO3, PO10, PSO1, PSO2
CO3	Analyze DSP processor architectures and hardware organization for efficient signal processing.	**L4**	PO1, PO2, PO10, PSO1, PSO2
CO4	Evaluate hardware implementation strategies and synthesis techniques for DSP algorithms.	**L5**	PO1, PO2, PO3, PO5, PO6, PO10, PO11, PSO1, PSO2
CO5	Design VLSI-based DSP systems using arithmetic units and optimized processing elements for real-time applications.	**L6**	PO1, PO2, PO3, PSO1, PSO2

REFERENCES:

1. *John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education,4th edition2019.*
2. *Keshab Parhi, "VLSI Digital Signal Processing Systems design &Implementation", JohnWiley &Sons,2007.*
3. *Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.*
4. *B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002..*
5. *Avtar Singh, S.Srinivasan, "Digital Signal Processing Implementations: Using DSP Microprocessors*
6. *(with examples from TMS320C54XX), Thomson Publications, 2004.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**3**	**2**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**3**	**3**	**-**
CO2	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**3**	**-**
CO3	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**-**	**3**	**2**	**-**
CO4	**2**	**3**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**2**	**2**	**3**	**2**	**-**
CO5	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**-**
25AEPE09	**3**	**3**	**3**	**-**	**2**	**2**	**-**	**-**	**-**	**3**	**2**	**3**	**3**	**-**

1-LOW 2-MODERATE (MEDIUM) 3- HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE10	Subject Title	RF SYSTEM DESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**Electronic devices, analog communication, analog integrated circuits, network theory, and microwave engineering** to understand RF front-end circuits, amplifiers, oscillators, mixers, and frequency synthesizers.		

OBJECTIVES:

- To introduce the principles of operation and design principles associated with the important blocks of RF Front end.
- To design RF amplifier, oscillators and mixers.
- To study about the characteristics of PLL and frequency synthesizers.

CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES (9 HOURS)

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject reciever, Low IF Receivers. Transmitter Architectures: Direct-conversion Transmitter, Heterodyne Transmitters.

IMPEDANCE MATCHING AND AMPLIFIERS (9 HOURS)

S-parameters with Smith chart, Passive IC components, Impedance matching networks, LNA topologies Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

FEEDBACK SYSTEMS AND POWER AMPLIFIERS (9 HOURS)

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Poweramplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MIXERS AND OSCILLATORS (9 HOURS)

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions,Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

PLL AND FREQUENCY SYNTHESIZERS (9 HOURS)

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequencysynthesizers, Direct Digital Frequency synthesizers.

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand RF transceiver specifications, receiver architectures, and transmitter architectures.	**L2**	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO3
CO2	Apply impedance matching techniques and amplifier design principles for RF circuits.	**L3**	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO3
CO3	Analyze the stability and performance of RF feedback systems and power amplifiers.	**L4**	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO3
CO4	Evaluate the characteristics and performance of RF mixers and oscillators.	**L5**	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO3
CO5	Design PLLs and frequency synthesizers for RF communication systems.	**L6**	PO1, PO2, PO3, PO4, PO5, PO9, PSO1, PSO3

REFERENCES:

1. *B.Razavi, "RF Microelectronics", 2nd Edition, Pearson, 2013.*
2. *B.Razavi, "Design of Analog CMOS Integrated Circuits",2nd Edition, McGraw Hill,2017.*
3. *Richard Chi-His Li, "RF Circuit Design", 2nd Edition, Wiley, 2012.*
4. *Pierre Baudin, "Wireless Transceiver Architecture: Bridging RF and DigitalCommunications",Wiley, 2014.*
5. *T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**
CO3	**3**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**
CO4	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**
CO5	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**
25AEPE10	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**1**

1-LOW 2-MODERATE (MEDIUM) 3- HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE11	Subject Title	SPEECH SIGNAL PROCESSING
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	**Digital signal processing, signals and systems, linear algebra, probability, and communication engineering** to understand speech analysis, audio coding, filter banks, and predictive speech processing techniques.		

OBJECTIVES:

- To studybasic concepts of processing speech signals.
- To studytime and frequency domain speech processing methods
- To understand predictive analysis of speech.

MECHANICS OF SPEECH AND AUDIO (9 HOURS)

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds– Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy - Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

TIME-FREQUENCY ANALYSIS: FILTER BANKSAND TRANSFORMS (9 HOURS)

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree- Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourierand Discrete Cosine Transform - Pre-echo Distortion- Pre- echo Control Strategies

AUDIO CODING AND TRANSFORM CODERS (9 HOURS)

Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding -Optimum Coding in the Frequency Domain - Perceptual Transform Coder – Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding – Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization - MDCT with Vector Quantization.

TIME AND FREQUENCY DOMAIN METHODSFOR SPEECH PROCESSING (9 HOURS)

Time domain parameters of Speech signal – Methods for extracting the parameters: Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

PREDICTIVE ANALYSIS OF SPEECH (9 HOURS)

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin‟s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP

TOTAL :45 PERIODS

Upon successful completion of this course, students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Understand the mechanics of speech production, auditory perception, and audio signal characteristics.	**L2**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3
CO2	Apply M-band filter banks and transform techniques for speech and audio signal processing.	**L3**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3
CO3	Analyze audio coding techniques and transform coders for efficient speech and audio compression.	**L4**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3
CO4	Evaluate time- and frequency-domain methods for speech parameter extraction and processing.	**L5**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3
CO5	Design predictive speech processing systems using linear prediction techniques and speech coding methods.	**L6**	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3

REFERENCES:

1. Lawrence Rabiner,biing and -Hwang Juang and B.Yegnanarayana Fundamaentals of Speech recognition,Pearson Education,2009

2. Ben Gold and Nelson Morgan, "Speech and Audio Signal Processing"; Processing andPerception of Speech and Music, Wiley-India Edition, 2006 .

3. L.R.Rabiner and R.W.Schaffer, "Introduction to Digital Signal Processing ,Foundations and Trends in Signal Processing Vol.1,Nos.1-2(2007)1-194.

4. UdoZölzer, "Digital Audio Signal Processing", Second Edition A John Wiley& sonsLtd,2008

5. Mark Kahrs,Karlheinz Brandebburg,Kluwer, "Applications of Digital Signal Processing to Audio and Acoustics",Academic Publishers.

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**2**	**2**	**2**	**2**	**2**	**2**	**1**	**1**	**3**	**1**	**2**	**2**	**1**	**2**
CO2	**2**	**2**	**2**	**2**	**2**	**3**	**1**	**1**	**3**	**1**	**2**	**2**	**2**	**2**
CO3	**2**	**2**	**2**	**3**	**3**	**3**	**1**	**1**	**3**	**1**	**2**	**3**	**3**	**2**
CO4	**2**	**2**	**2**	**3**	**3**	**3**	**1**	**1**	**3**	**1**	**2**	**3**	**3**	**2**
CO5	**2**	**2**	**2**	**3**	**3**	**3**	**1**	**1**	**3**	**1**	**2**	**3**	**3**	**2**
25AEPE11	**2**	**2**	**2**	**3**	**3**	**3**	**1**	**1**	**3**	**1**	**2**	**3**	**3**	**2**

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE12	Subject Title	SOLID STATE DEVICE MODELLING AND SIMULATION
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Basic knowledge of Semiconductor Devices, Electronic Devices & Circuits, Network Analysis, Engineering Mathematics (Differential Equations, Linear Algebra), and Fundamentals of VLSI Design.		

OBJECTIVES:

- To studyphysics of MOSFET devices.
- To understand the concept of device modelling.
- To study mathematical techniques of device simulations.

MOSFET DEVICE PHYSICS MOSFET (9 HOURS)

capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors,Inductors.

DEVICE MODELLING (9 HOURS)

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques,solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

MULTISTEP METHODS (9 HOURS)

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

MATHEMATICAL TECHNIQUES DEVICESIMULATIONS (9 HOURS)

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation,hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

SIMULATION OF DEVICES (9 HOURS)

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the physics, operation, characteristics, and equivalent circuit models of MOS capacitors and MOSFETs, including small-signal and high-frequency behavior.	L2	PO1, PO2, PO3, PO5
CO2	Apply device modeling techniques, network analysis methods, and numerical approaches such as Newton–Raphson and sparse matrix techniques to solve electrical network equations.	L3	PO1, PO2, PO3, PO4, PO5
CO3	Analyze semiconductor device equations, including Poisson, continuity, drift–diffusion, Schrödinger, and hydrodynamic equations, for device simulation.	L4	PO1, PO2, PO4, PO5
CO4	Develop simulation models for MOSFETs and other semiconductor devices using multistep numerical methods and finite difference techniques.	L3	PO2, PO3, PO4, PO5

CO5	Evaluate compact device models and simulation results for semiconductor devices by interpreting model parameters and assessing device characteristics.	**L5**	**PO1, PO2, PO4, PO5, PO10**

REFERENCES:

1. *Arora, N., "MOSFET Modeling for VLSI Simulation", Cadence DesignSystems,2007*
2. *Modeling and Simulation in Engineering Edited by Jan Valdman and Leszek Marcinkowski,published by 2020*
3. *Grasser, T., "Advanced Device Modeling and Simulation", World ScientificPublishing Company.,2003*
4. *The Physics and Modeling of Mosfets- June 2008 Mitiko Miura-Mattausch (Hiroshima University, Japan), Hans Jürgen Mattausch(Hiroshima University,Japan), and Tatsuya Ezaki (Hiroshima University, Japan)*
5. *F. John Dian," Fundamentals of Internet of Things: For Students and Professionals",Wiley, 2022.Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modelingfor Analog and RFCMOS Circuit Design", John Wiley &Sons Ltd.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO2	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO3	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO4	3	3	3	3	3	2	2	-	-	3	-	2	3	2
CO5	3	3	3	3	3	2	2	-	-	3	-	2	3	2
25AEPE12	3	3	3	3	3	2	2	-	-	3	-	2	3	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

GOVERNMENT COLLEGE OF ENGINEERING, BARGUR
(An Autonomous Institution Affiliated to Anna University)
M.E. APPLIED ELECTRONICS

Subject Code	25AEPE13	Subject Title	ADVANCED MICROPROCESSOR AND MICROCONTROLLER ARCHITECTURES
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Microprocessors and Microcontrollers, Assembly Language Programming		

OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture
- To familiarize the high performance features in RISC architecture
- To introduce the basic features in Motorola microcontrollers.
- To study interfacing of microprocessor/microcontroller with the external peripheral

MICROPROCESSOR ARCHITECTURE (9 HOURS)

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards –instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

HIGH PERFORMANCE CISC ARCHITECTURE –PENTIUM (9 HOURS)

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set –addressingmodes – Programming the Pentium processor.

HIGH PERFORMANCE RISC ARCHITECTURE –ARM (9 HOURS)

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

MSP430 16 - BIT MICROCONTROLLER (9 HOURS)

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 -DevelopmentTools, ADC - PWM - UART - Timer Interrupts - System design using MSP430 Microcontroller.

HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES (9 HOURS)

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-M3 architecture

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of microprocessor architecture, instruction formats, addressing modes, memory hierarchy, pipelining, and RISC–CISC concepts.	**L2**	**PO1, PO2, PO3**
CO2	Apply the instruction set, addressing modes, and programming techniques of the Pentium processor to solve CISC-based computing problems.	**L3**	**PO1, PO2, PO3, PO5**
CO3	Analyze the architecture, memory management, instruction set, and programming model of ARM RISC processors for embedded applications.	**L4**	**PO1, PO2, PO3, PO4**
CO4	Evaluate the performance and functionality of MSP430 microcontroller peripherals and ARM Cortex-M3 architecture for embedded system design.	**L5**	**PO1, PO2, PO4, PO5**
CO5	Design embedded system solutions using ARM Cortex-M3/MSP430 microcontrollers by integrating appropriate peripherals and programming techniques.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO10**

REFERENCES:

1. *Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 2005*
2. *Pearson Prentice Hall Language:English Author:Barry B. Brey 2009.*
3. *Steve Furber , „" ARM System –On –Chip architecture "Addision Wesley , 2000.*
4. *Gene .H.Miller ." Micro Computer Engineering ," Pearson Education ,4th edition 2015.*
5. *Joseph Yiu, "The Definitive Guide to the ARM ® Cortex-M3", Newnes, 2013..*
6. *John H.Davis , "MSP 430 Micro controller basics", Eelsevier, 2015.*
7. *James L.Antonako, "An Introduction to the Intel family of Microprocessors", Pearson Education2014.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	2	-	-	3	-	2	2	2	3
CO2	3	2	2	2	-	3	-	-	3	-	2	2	2	3
CO3	3	2	2	2	-	3	-	-	3	-	2	3	2	3
CO4	3	2	2	2	-	3	-	-	3	-	2	3	2	3
CO5	3	2	2	2	-	3	-	-	3	-	2	3	2	3
25AEPE13	3	2	2	2	-	3	-	-	3	-	2	3	2	3

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE14	Subject Title	SYSTEM ON CHIP
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Computer Organization and Architecture, Embedded Systems		

OBJECTIVES:

- To introduce the architectural features of system on chip.
- To imbibe the knowledge of customization using case studies.
- To studythe Challenges on SOC hardware and software.

INTRODUCTION TO THE SYSTEM APPROACH (9 HOURS)

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

PROCESSORS (9 HOURS)

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays,Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors,Superscalar Processors.

MEMORY DESIGN FOR SOC (9 HOURS)

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

INTERCONNECT CUSTOMIZATION (9 HOURS)

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization

CONFIGURATION (9 HOURS)

An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor,Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the architecture, components, design methodology, and complexity of System-on-Chip (SoC) design.	**L2**	**PO1, PO2, PSO1**
CO2	Apply processor selection criteria and analyze processor architectures, pipelines, superscalar, VLIW, and vector processors for SoC applications.	**L3**	**PO1, PO2, PO3, PO4, PSO1**
CO3	Analyze memory hierarchy, cache organization, virtual memory, and processor–memory interactions in SoC architectures.	**L4**	**PO1, PO2, PO3, PO4, PSO1, PSO2**
CO4	Evaluate SoC interconnection architectures, standard buses, and customization techniques based on performance and communication requirements.	**L5**	**PO1, PO2, PO4, PO6, PSO1**
CO5	Design configurable and reconfigurable SoC-based systems by selecting suitable processor customization and reconfiguration techniques for specific applications.	**L6**	**PO1, PO2, PO3, PO6, PSO1, PSO2**

REFERENCES:

1. *Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk,Wiely India Pvt. Ltd.2011.*
2. *Abderazek Ben Abdallah,- Advanced Multicore Systems-On-Chip, Architecture, On-Chip Network, Design ©*
3. *Springer Nature Singapore Pte Ltd. 2017.*
4. *CRC Press is an imprint of Taylor & Francis Group, an Informa business Network-on-Chip, The NextGeneration*
5. *of System-on-Chip Integration by Santanu Kundu, Santanu Chattopadhyay, © 2015.*
6. *Pasricha – Nikil Dutt "On-Chip Communication Architectures System on ChipInterconnect" by SudeepMorgan*
7. *Kaufmann Publishers, © 2008 Elsevier, Inc.*
8. *Multiprocessor System-on-Chip: Hardware Design and Tool Integration, by MichaelHubner l Jurgen*
9. *Becker Editors # Springer Science + Business Media, LLC 2011..*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	-	1	-	-	-	-	-	-	-	3	1	1
CO2	3	2	2	2	-	2	-	-	-	-	-	3	2	1
CO3	3	3	3	1	-	-	-	-	-	-	-	3	2	2
CO4	2	3	-	2	-	1	-	-	-	-	-	3	1	2
CO5	3	3	2	-	-	1	-	-	-	-	-	3	2	2
25AEPE14	3	3	2	1	-	1	-	-	-	-	-	3	2	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE15	Subject Title	ROBOTICS AND INTELLIGENT SYSTEMS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Programming Fundamentals, and Artificial Intelligence concepts.		

OBJECTIVES:

- To Teach the basic concepts in robotics.
- To expose the various design aspects in robot grippers.
- To make learn various drives and control systems.
- To impart knowledge on machine vision systems.
- To applyrobot based concepts for automation

INTRODUCTION (9 HOURS)

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, dexterity, RCC device. Automation-Concept, introduction to automation productivity, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations.

ROBOT GRIPPERS (9 HOURS)

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

DRIVES AND CONTROL SYSTEMS (9 HOURS)

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control . Control Technologies in Automation:- Control System Components such as Sensors, Actuators and others. Industrial Control Systems , Continuous Verses Discrete Control, Process industries Verses Discrete -Manufacturing Industries.

MACHINE VISION SYSTEM (9 HOURS)

Vision System Devices, Robot Programming :- Methods of robot programming, lead through programming, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION (9 HOURS)

Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, robots and application of robots for automation. Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updates in robotics.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of robotics, automation, robot anatomy, classifications, and industrial applications of robotic systems.	**L2**	**PO1, PO2, PO3, PSO1**
CO2	Apply the principles of robot grippers, sensors, actuators, and control systems in the design and operation of robotic subsystems.	**L3**	**PO1, PO2, PO3, PO5, PSO1**
CO3	Analyze robot drive mechanisms, control strategies, machine vision systems, and robot programming techniques for industrial automation.	**L4**	**PO1, PO2, PO4, PO5, PSO2**
CO4	Evaluate manufacturing automation systems using mathematical models, artificial intelligence techniques, and robotic technologies.	**L5**	**PO1, PO2, PO4, PO5, PO10, PSO2**
CO5	Design intelligent robotic solutions for automation by integrating machine vision, AI techniques, and modern robotic technologies to address industrial applications.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO10, PSO1, PSO2**

REFERENCES:

1. *John J. Craig," Introduction to Robotics (Mechanics and Control)", 2014.*
2. *Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming andApplications", McGraw-Hill 2012.*
3. *Bruno Siciliano, Oussama khatib, " Springer Handbook of Robotics" ,2016.*
4. *Automation, "Production Systems and Computer Integrated Manufacturing", M.P.Groover,Pearson Education 2008.*
5. *Laxmidhar Behera, Swagat kumar, Prem kumar patchaikani , Ranjith RavindranathanNair, Samrat Dutta "Intelligent control of Robotics Systems",2020*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3	1	2	-	-	-	-	3	2	3	2	2
CO2	2	2	1	-	2	-	-	-	-	2	3	2	3	2
CO3	2	1	-	2	2	-	-	-	-	3	2	2	2	1
CO4	2	2	1	2	2	-	-	-	-	2	2	3	2	2
CO5	3	2	1	2	1	-	-	-	-	2	2	3	2	1
25AEPE15	2	2	1	2	2	-	-	-	-	2	2	3	2	2

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE16	Subject Title	PHYSICAL DESIGN OF VLSI CIRCUITS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Computer-Aided Design (CAD), and Electronic Circuits.		

OBJECTIVES:

- To introduce the physical design concepts such as layout rules, circuit abstraction, layout methodologies and packaging.
- To study placement of design using top down approach.
- To study the performance of circuits layout designs, compaction techniques.

INTRODUCTION TO VLSI TECHNOLOGY (9 HOURS)

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array (FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms

PLACEMENT USING TOP-DOWN APPROACH (9 HOURS)

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

ROUTING USING TOP DOWN APPROACH (9 HOURS)

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow-based techniques – Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

PERFORMANCE ISSUES IN CIRCUIT LAYOUT (9 HOURS)

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

SINGLE LAYER ROUTING, CELL GENERATIONAND COMPACTION (9 HOURS)

Planar subset problem (PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over the Cell (OTC) Routing Multiple chip modules (MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout-1Dcompaction- 2D compaction.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of VLSI physical design, layout methodologies, design rules, programmable logic arrays, FPGA architecture, and packaging techniques.	**L2**	**PO1, PO2, PSO1**
CO2	Apply partitioning, floor planning, and placement algorithms using top-down design methodologies for VLSI physical design.	**L3**	**PO1, PO2, PO3, PO4, PSO1**
CO3	Analyze global and detailed routing techniques, including FPGA routing methods, to optimize interconnections in VLSI circuits.	**L4**	**PO1, PO2, PO3, PO4, PSO1, PSO2**
CO4	Evaluate circuit layout performance using delay models, timing-driven placement, routing strategies, and via minimization techniques.	**L5**	**PO1, PO2, PO4, PO10, PO11**
CO5	Design optimized VLSI layouts using single-layer routing, compaction techniques, and cell generation methods for efficient physical implementation.	**L6**	**PO1, PO2, PO3, PO4, PO10, PSO1, PSO2**

REFERENCES:

1. *AndrewB.Kahng " VLSI physical Design" 2011*
2. *Naveed A.Sherwani " VLSI Physical Design Automation" 2012*
3. *Liming Xiu "VLSI circuit Design Methodology Demystified" 2007*
4. *Hubert Kaeslin "Top- Down Digital VLSI Design"2014.*
5. *M.Michael Vai "VLSI Design "2017.*

COURSE ARTICULATION MATRIX

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	1	1	2	_	_	2	_	2	2	2	1	1	2
CO2	3	2	2	3	_	_	2	_	2	1	2	2	2	2
CO3	3	1	1	2	_	_	2	_	2	2	2	1	1	2
CO4	3	1	1	1	_	_	2	_	2	2	2	1	1	2
CO5	2	1	1	2	_	_	1	_	2	2	2	1	1	2
25AEPE16	3	2	1	2	_	_	2	_	2	2	2	1	1	2

1- Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE17	Subject Title	HIGH PERFORMANCE NETWORKS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Probability and Statistics, and Network Security fundamentals.		

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networking
- To introduce high speed switching concepts
- Realize the concept of Internet of Things in the real-world scenario
- To studythe types of VPN and tunneling protocols for security
- To learn about network security in many layers and network management

INTRODUCTION (9 HOURS)

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET –DWDM –DSL – ISDN – BISDN, ATM.

MULTIMEDIA NETWORKING APPLICATIONS (9 HOURS)

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications –Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

ADVANCED NETWORKS CONCEPTS (9 HOURS)

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, and MPLS based VPN,overlay networks- P2P connections.

TRAFFIC MODELLING (9 HOURS)

Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models,Network performance evaluation.

NETWORK SECURITY AND MANAGEMENT (9 HOURS)

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and fire walls – attacks and counter measures – security in many layers. Infrastructure for networkmanagement – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of high-performance networks, communication technologies, switching, routing, multiplexing, and high-speed networking standards.	L2	PO1, PO2, PSO1
CO2	Apply multimedia networking protocols, quality of service (QoS) mechanisms, integrated services, and differentiated services for real-time network applications.	L3	PO1, PO2, PO3, PO4, PSO1
CO3	Analyze VPN architectures, MPLS, tunneling protocols, and overlay networks to support secure and efficient communication.	L4	PO1, PO2, PO3, PO4, PSO1
CO4	Evaluate network traffic models and performance using mathematical techniques and queueing theory for high-performance network analysis.	L5 –	PO1, PO2, PO4, PO10
CO5	Design secure and manageable network solutions by integrating cryptographic techniques, authentication mechanisms, firewalls, and network management protocols.	L6	PO1, PO2, PO3, PO4, PO5, PO10, PSO1

REFERENCES:

1. *Aunurag Kumar, D. M Anjunath, Joy Kuri, "Communication Networking", MorganKaufmann Publishers, 1st edition 2004.*
2. *Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet",Pearson education, 5th edition-2006.*
3. *J.F.Kurose & K.W.Ross, "Computer Networking-A top down approach featuringtheinternet", Pearson, 3rd edition,2005.*
4. *Gerry Howser,"Computer Networking and the Internet", Springer,2020.*
5. *Nader F.Mir, "Computer and Communication Networks", Pearson Education- 1st edition2010.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	1	-	-	2	2	2	-	-	2	1	1
CO2	2	2	1	1	-	-	2	2	-	-	-	2	1	-
CO3	3	2	-	1	-	-	1	2	2	-	-	2	-	-
CO4	3	3	1	3	-	-	2	3	-	-	-	-	-	1
CO5	2	2	-	2	-	-	2	2	-	-	-	-	-	-
25AEPE17	3	2	-	1	-	-	2	2	-	-	-	2	-	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE18	Subject Title	PATTERN RECOGNITION
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Basics of Machine Learning and Digital Image Processing		

OBJECTIVES:

- To introduce the fundamentals of pattern recognition techniques
- To understand various clustering techniques
- To introduce sequential pattern recognition methods
- To introduce the concepts of support vector machines
- To introduce the fundamentals of neural networks

PATTERN CLASSIFICATION (9 HOURS) 9

Overview of pattern recognition, Supervised learning. Bayes decision theory, Minimum-error-rate classification, Classifiers, Discriminant functions, and Decision surfaces. Normal density(univariate and multivariate) and discriminant functions for the normal density. Discrete features. Parameter estimation methods: Maximum likelihood estimation, Maximum a posteriori estimation. Bayesian estimation:Gaussian case. Pattern classification by distance functions - minimumdistance classifier.

CLUSTERING (9 HOURS) 9

Unsupervised learning and clustering - criterion functions for clustering. Algorithms for clustering -k- means and hierarchical clustering, Cluster validation. Expectation-maximization algorithm.Gaussian mixture models, model selection for latent variable models, high-dimensional spaces, the curse of dimensionality, dimensionality reduction, factor analysis, Principal component analysis, probabilisticPCA,Independent component analysis.

PROBABILISTIC GRAPHICAL MODELS (9 HOURS) 9

Directed graphical models - Bayesian network. From distributions to graphs - examples-Markov Random fields-inference in graphical models - Markov model - Hidden Markov Models (HMMs) - building ahidden Markov model for multi-class pattern recognition, issues.

SUPPORT VECTOR MACHINES (9 HOURS) 9

Constrained optimization problems - linearly separable and non-separable patterns, hyper plane andmargin -discriminant function of a hyper plane, maximum margin hyper plane. Kernel functions - vector kernels - linear, polynomial and Gaussian kernels, non-vector kernels. Building a support- vector machine for multi-class pattern recognition - architecture, choice of kernels, issues.

ARTIFICIAL NEURAL NETWORKS (9 HOURS) 9

Models of a neuron - feed-forward neural networks - Perceptron learning, Multi-layer feed-forward neural network, Gradient descent, back propagation algorithm - network pruning, limitations and convergence of back-propagation learning. Cover's theorem on the separability of patterns, Generalized radial-basis function networks, Auto encoder networks - auto- association neural network - convolutional neural network.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of pattern recognition, Bayesian decision theory, discriminant functions, and statistical classification techniques.	**L2**	**PO1, PO2, PO5, PSO1**
CO2	Apply clustering algorithms, dimensionality reduction techniques, and probabilistic models for pattern analysis and feature extraction.	**L3**	**PO1, PO2, PO3, PO4, PO5, PSO1**
CO3	Analyze probabilistic graphical models, Hidden Markov Models (HMMs), and Support Vector Machines (SVMs) for solving pattern recognition problems.	**L4**	**PO1, PO2, PO3, PO4, PO5, PSO1**
CO4	Evaluate the performance of classification models using kernel methods, SVM architectures, and neural network learning algorithms for pattern recognition applications.	**L5**	**PO1, PO2, PO4, PO5, PO10, PSO2**
CO5	Design intelligent pattern recognition systems using artificial neural networks, autoencoders, and convolutional neural networks for real-world applications.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO10, PSO1, PSO2**

REFERENCES:

1. *Duda R.O, Hart P.E. and Stork D.G, "Pattern Classification", John Wiley, 2nd Edition2009.*
2. *Bishop C.M, "Pattern Recognition and Machine Learning", Springer-1st Edition-2006*
3. *Theodoridis S and Koutroumbas K, "Pattern Recognition", Elsevier-4th Edition-2009.*
4. *Simon Haykin, "Neural networks- a comprehensive foundation ", Pearson Education,2nd Edition-2008.*
5. *Joao Luis G. Rosa,"Artificial Neural Networks-Models and Applications", IN-TECH,2016.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	-	2	-	-	3	-	2	-	2	2	-	-	1	2
CO2	2	2	-	3	2	-	-	2	-	1	2	2	1	-
CO3	3	2	2	1	2	2	-	1	2	-	-	2	1	-
CO4	3	3	1	2	2	1	-	2	-	2	2	1	2	1
CO5	2	2	1	2	-	-	2	1	1	-	1	2	2	1
25AEPE18	3	2	1	1	2	1	2	2	1	2	1	2	1	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE19	Subject Title	SECURE COMPUTING SYSTEMS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Programming in C/C++, Data Structures, and Information Security fundamentals.		

OBJECTIVES:

- To learn different computer security mechanism and management techniques.
- To gain knowledge about computer hardware security.
- To applyprogramming knowledge in hardware.

COMPUTER SECURITY AND MANAGEMENT (9 HOURS)

Overview of Computer Security, Threats, Malware, Vulnerabilities, Authentication, Access Control, SecurityManagement Models, Security Management Practices, Protection Mechanisms, Legal aspects of security, Ethical Hacking.

HARDWARE SECURITY (9 HOURS)

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Countermeasures of Side Channel Attack, Secure Hardware Intellectual Properties, Physically Unclonable Functions (PUFs), Secure PUF.

ASSEMBLY AND OPERATING SYSTEMS SECURITY (9 HOURS)

Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions

ADVANCED COMPUTER ARCHITECTURE (9 HOURS)

Security aspects: Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization

NETWORK AND WEB SECURITY (9 HOURS)

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamental concepts of computer security, security management, authentication, access control, threats, vulnerabilities, and protection mechanisms.	**L2**	**PO1, PO2, PO6, PSO2**
CO2	Apply hardware security techniques, secure hardware design principles, physically unclonable functions (PUFs), and countermeasures against side-channel attacks.	**L3**	**PO1, PO2, PO3, PO5, PO6, PSO2**
CO3	Analyze security issues in assembly language, operating systems, advanced computer architectures, cloud computing, virtualization, and distributed systems.	**L4**	**PO1, PO2, PO3, PO5, PO6, PO11, PSO2**
CO4	Evaluate security mechanisms for computer systems, networks, and web-based applications by assessing	**L5**	**PO1, PO2, PO5, PO6, PO11, PSO2**

	vulnerabilities, trusted system functions, and secure computing environments.		
CO5	Design secure computing solutions by integrating hardware, operating system, network, and system-level security mechanisms to address organizational security requirements.	**L6**	**PO1, PO2, PO3, PO5, PO6, PO11, PSO2**

REFERENCES:

1. *Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", Fourth Edition, Pearson Education, 2007*
2. *Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security – Design Threats and Safeguards", CRC Press, 2015*
3. *Michael Whitman, Herbert J. Mattord, "Management of Information Security", Third Edition, CourseTechnology, 2010*
4. *Shuangbao Wang, Robert S.Ledley, Computer Architecture and Security, Wiley, 2013*
5. *William Stallings, "Network Security Essentials, Applications and Standards", Dorling Kindersley I PLtd, Delhi, 2008.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	-	-	1	2	-	-	-	-	1	-	2	-
CO2	2	2	2	-	1	2	-	-	2	-	2	-	2	-
CO3	3	1	1	-	3	3	-	-	1	-	2	-	2	-
CO4	3	2	-	-	2	2	-	-	2	-	3	-	2	-
CO5	2	-	2	-	2	3	-	2	2	-	2	-	2	-
25AEPE19	2	2	2	-	2	2	-	-	2	-	2	-	2	-

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE20	Subject Title	SIGNAL INTEGRITY FOR HIGH SPEEDDESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Basic knowledge of Electromagnetic Fields, Analog and Digital Electronics		

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

SIGNAL PROPAGATION ON TRANSMISSION LINES (9 HOURS)

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cuthicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section,reflection coefficient, skin- effect, dispersion

MULTI-CONDUCTOR TRANSMISSION LINES ANDCROSS-TALK (9 HOURS)

Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk,minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits, S- parameters, Lossy and Lossles models.

NON-IDEAL EFFECTS (9 HOURS)

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ, routing parasitic, Common-mode current, differential-mode current, Connectors

POWER CONSIDERATIONS AND SYSTEM DESIGN (9 HOURS)

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

CLOCK DISTRIBUTION AND CLOCK OSCILLATORS (9 HOURS)

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of signal propagation, transmission line theory, impedance matching, reflections, and termination techniques in high-speed digital systems.	L2	PO1, PO2, PSO1
CO2	Apply transmission line models, differential signaling techniques, and crosstalk reduction methods to improve signal integrity in high-speed interconnects.	L3	PO1, PO2, PO3, PO4, PSO1

CO3	Analyze the impact of parasitic effects, transmission line losses, common-mode noise, and connector characteristics on signal integrity performance.	**L4**	**PO1, PO2, PO3, PO4, PSO1, PSO2**
CO4	Evaluate power distribution networks, simultaneous switching noise (SSN), package parasitics, timing analysis, eye diagrams, and bit-error rate for reliable high-speed system design.	**L5**	**PO1, PO2, PO3, PO4, PO10, PO11**
CO5	Design robust clock distribution networks and high-speed digital systems by incorporating clock synchronization, jitter reduction, delay optimization, and signal integrity design practices.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO10, PSO1, PSO2**

REFERENCES:

1. *H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of BlackMagic, Prentice Hall,2010*
2. *Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice HallPTR , 2012.*
3. *S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook ofInterconnect Theory and Design Practices, Wiley-Interscience, 2014..*
4. *Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2013.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	_	_	2	_	2	2	2	1	1	2
CO2	3	3	3	3	_	_	2	_	2	1	2	2	2	2
CO3	3	2	2	2	_	_	1	_	2	1	2	1	1	2
CO4	3	3	3	3	_	_	2	_	2	1	2	2	2	2
CO5	3	2	2	2	_	_	2	_	1	2	2	1	1	2
25AEPE20	3	2	2	2	_	_	2	_	2	1	2	1	1	2

1- Low 2—Moderate (Medium) 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE21	Subject Title	WIRELESS AD-HOC AND SENSOR NETWORKS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Operating Systems, and Network Security fundamentals.		

OBJECTIVES:

- To study the ADHOC networks and its protocols
- To implement the designing of multicast routing and security
- To study the Challenges in QOS and power management schemes

MAC & ROUTING IN AD HOC NETWORKS (9 HOURS)

Introduction – Issues and challenges in ad hoc networks – MAC Layer Protocols for wireless ad hoc networks – Contention-Based MAC protocols – MAC Protocols Using Directional Antennas – Multiple- Channel MAC Protocols – Power-Aware MAC Protocols – Routing in Ad hoc Networks – Design Issues – Proactive, Reactive and Hybrid Routing Protocols

TRANSPORT & QOS IN AD HOC NETWORK (9 HOURS)

TCP's challenges and Design Issues in Ad Hoc Networks – Transport protocols for ad hoc networks – Issues and Challenges in providing QoS – MAC Layer QoS solutions – Network Layer QoS solutions –QoS Model

MAC & ROUTING IN WIRELESS SENSOR NETWORKS (9 HOURS)

Introduction – Applications – Challenges – Sensor network architecture – MAC Protocols for wireless sensor networks – Low duty cycle protocols and wakeup concepts – Contention- Based protocols – Schedule-Based protocols – IEEE 802.15.4 Zigbee – Topology Control – Routing Protocols

TRANSPORT & QOS IN WIRELESS SENSOR NETWORKS (9 HOURS)

Data-Centric and Contention-Based Networking – Transport Layer and QoS in Wireless Sensor Networks – Congestion Control in network processing – Operating systems for wireless sensor networks – Examples

SECURITY IN AD HOC AND SENSOR NETWORKS (9 HOURS)

Security Attacks – Key Distribution and Management – Intrusion Detection – Software based Anti-tamper techniques – Water marking techniques – Defence against routing attacks - Secure Ad hoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of wireless ad-hoc and sensor networks, including MAC protocols, routing techniques, and network architecture.	L2	PO1, PO2, PSO1
CO2	Apply routing protocols and transport layer mechanisms to design efficient communication in ad-hoc networks.	L3	PO1, PO2, PO3, PO4, PSO1
CO3	Analyze MAC protocols, QoS mechanisms, and design issues in wireless ad-hoc and sensor networks.	L4	PO1, PO2, PO3, PSO1, PSO2
CO4	Evaluate routing strategies, congestion control, and QoS performance in wireless sensor networks using appropriate metrics.	L5	PO1, PO2, PO3, PO4, PO6, PSO1, PSO2

CO5	Design secure ad-hoc and sensor network systems by implementing security protocols, intrusion detection, and key management techniques.	**L6**	**PO1, PO2, PO3, PO6, PSO1, PSO2**

REFERENCES:

1. *Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks:Theory and Applications (2nd Edition), World Scientific Publishing, 2011*
2. *Waltenegus Dargie, Christian Poellabauer, —Fundamentals of Wireless Sensor NetworksTheory and Practice, John Wiley and Sons, 2010*
3. *Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, —Ad Hoc Mobile Wireless Networks‖, Auerbach Publications, 2008.*
4. *C.Siva Ram Murthy and B.S.Manoj, —Ad Hoc Wireless Networks – Architectures and 2Protocols‖, Pearson Education, 2006.*
5. *Holger Karl, Andreas Willing, —Protocols and Architectures for Wireless Sensor Networks‖, John Wiley& Sons, Inc., 2005.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	-	1	-	-	-	-	-	-	-	3	1	1
CO2	3	2	2	2	-	2	-	-	-	-	-	3	2	1
CO3	3	3	3	1	-	-	-	-	-	-	-	3	2	2
CO4	2	3	-	2	-	1	-	-	-	-	-	3	1	2
CO5	3	3	2	-	-	1	-	-	-	-	-	3	2	2
25AEPE21	3	3	2	1	-	1	-	-	-	-	-	3	2	2

1- LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25AEPE22	Subject Title	HARDWARE - SOFTWARE CO-DESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Operating Systems, and VLSI Design fundamentals.		

OBJECTIVES:

- To acquire the knowledge about system specification and modeling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation.

SYSTEM SPECIFICATION AND MODELLING (9 HOURS)

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modelling, Co- Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

HARDWARE / SOFTWARE PARTITIONING (9 HOURS)

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

HARDWARE / SOFTWARE CO-SYNTHESIS (9 HOURS)

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation,Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

PROTOTYPING AND EMULATION (9 HOURS)

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems

DESIGN SPECIFICATION AND VERIFICATION (9 HOURS)

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi- Language Co- simulation.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain system specification, modeling techniques, embedded system architectures, and hardware/software co-design methodologies.	L2	PO1, PO2, PO3, PSO1
CO2	Apply hardware/software partitioning techniques using cost estimation, heuristic scheduling, and optimization approaches.	L3	PO1, PO2, PO3, PSO1, PSO2

CO3	Analyze hardware/software co-synthesis methods including state-transition models, controller generation, and distributed system design.	**L4**	**PO1, PO2, PO3, PO11, PSO1, PSO2**
CO4	Evaluate prototyping and emulation techniques for different target architectures and embedded system application classes.	**L5**	**PO1, PO2, PO6, PO8, PSO1, PSO2**
CO5	Design and verify system-level hardware/software co-design solutions using specification languages, concurrency models, and co-simulation tools.	**L6**	**PO1, PO2, PO3, PO4, PO6, PO8, PSO1, PSO2**

REFERENCES:

1. *Joris van den Hurk,JochenA.G.Jess "System Level Hardware/Software Co-Design2013*
2. *Jorgen Staunstrup , Wayne wolf "Hardware and software Co-Design ",2007*
3. *Patrick R. Schaumount "A practical introduction to Hardware/Softwarecodesign"2010*
4. *Soonhoi Ha,Jorgen Teich"Handbook of Hardware/ Software codesign"2017*
5. *Sao-Jie Chen, Guang - Huei Lin, Pao-Ann Hsiung ,Yu-Hen Hu" Hardware/Softwarecodesign of Multimedia SOC platform" 2009.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	3	2	-	-	-	-	-	-	-	3	2	1
CO2	1	3	2	2	-	-	-	-	-	-	-	3	2	1
CO3	1	2	2	-	-	-	-	-	-	-	1	2	2	1
CO4	3	2	-	-	-	2	-	1	-	-	-	2	2	1
CO5	3	2	3	3	-	2	-	1	-	-	-	3	2	1
25AEPE22	2	2	2	2	-	1	-	1	-	-	-	3	2	1

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEPE23	Subject Title	PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	I & II
Prerequisites	Operating Systems, and Embedded Systems fundamentals.		

OBJECTIVES:

- To make students familiar with the basic concepts embedded software.
- To foster ability to understand the design concept of object-oriented programming techniques
- To explain programming concepts and embedded programming in c and C++
- Ability to understand the role of scripting languages in embedded software

EMBEDDED 'C' (9 HOURS)

Programming Bitwise operations, Dynamic memory allocation, OS services Linked list, stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Writing LCD drives, LED drivers, Drivers forserial port communication. Embedded Software Development Cycle & Methods (Waterfall, Agile).

OBJECT ORIENTED PROGRAMMING (9 HOURS)

Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.

CPP PROGRAMMING (9 HOURS)

'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.

OVERLOADING AND INHERITANCE (9 HOURS)

Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance,multiple inheritance, virtual base class, polymorphism, virtual functions.

TEMPLATES (9 HOURS)

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. **Scripting Languages :** Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain embedded C programming concepts including data structures, interrupt handling, device drivers, and software development methodologies.	L2	PO1, PO2, PO3, PSO1
CO2	Apply object-oriented programming principles to design modular and reusable software solutions for embedded systems.	L3	PO1, PO2, PO3, PSO1

CO3	Analyze C++ programming constructs including classes, constructors, destructors, and memory management techniques for software development.	**L4**	**PO1, PO2, PO3, PO11, PSO1, PSO2**
CO4	Evaluate advanced object-oriented features such as inheritance, polymorphism, and operator overloading for efficient embedded software design.	**L5**	**PO1, PO2, PO4, PO6, PSO1, PSO2**
CO5	Design embedded software solutions using templates, exception handling, and scripting languages for real-world applications.	**L6**	**PO1, PO2, PO3, PO4, PO6, PO8, PSO1, PSO2**

REFERENCES:

1. *Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2015 reprint*
2. *Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011.*
3. *A. Michael Berman, "Data structures via C++", Oxford University Press, 2002..*
4. *Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999.*
5. *braham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey &Sons, 2005.*

COURSE ARTICULATION MATRIX:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	**2**	**3**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**1**
CO2	**1**	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**1**
CO3	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**	**1**
CO4	**3**	**2**	**-**	**-**	**-**	**2**	**-**	**1**	**-**	**-**	**-**	**2**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**-**	**2**	**-**	**1**	**-**	**-**	**-**	**3**	**2**	**1**
25AEPE23	**2**	**2**	**2**	**2**	**-**	**1**	**-**	**1**	**-**	**-**	**-**	**3**	**2**	**1**

1-LOW 2-MODERATE (MEDIUM) 3-HIGH

Course Designed By

Name & Designation **BOS Approval**

Date:

OPEN ELECTIVES

Subject Code	25AEOE01	Subject Title	AUTOMOTIVE ELECTRONIC SYSTEMS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	III
Prerequisites	Automotive Engineering fundamentals, Electronics, Sensors and Transducers		

OBJECTIVES:

- Describe the basics of automobile dynamics and design electronics.
- Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's
- automotive industry
- Design and implement the electronics that attribute the reliability, safety and smartness to the automobiles,
- providing add-on comforts and get fair idea on future Automotive Electronic Systems.

ELECTRONIC ENGINE CONTROL SYSTEM (9 HOURS)

Motivation for Electronic Engine Control- Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure.

SENSORS AND ACTUATORS (9 HOURS)

Basic sensor arrangement, Types of sensors such as-Oxygen sensors, Crank angle position sensors-Fuel metering/vehicle speed sensor and detonation sensor- Altitude sensor, flow sensor. Throttle position sensors. Solenoids, stepper motors, and relays.

VEHICLE MOTION CONTROL SYSTEM (9 HOURS)

Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Antilock Brake System (ABS). Electronic suspension, electronic steering control, and traction control.

ELECTRONIC FUEL INJECTION AND IGNITION SYSTEM (9 HOURS)

Feedback carburetor systems. Throttle body injection and multiport or point fuel injection, fuel injection systems, Injection system controls. Advantages of electronic ignition systems: Types of solid-state ignition systems and their principle of operation, Contact less electronic ignition system and electronic spark timing control.

DIGITAL ENGINE CONTROL SYSTEM (9 HOURS)

Open loop and closed loop control systems-Engine cranking and warm up control-Acceleration enrichment- Deceleration leaning and idle speed control. Distributor less ignition-Integrated engine control systems, Exhaust mission control engineering. Electronic dashboard instruments Onboard diagnosis system, security and warning system.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals of automotive systems, engine performance parameters, electronic engine control concepts, and emission control strategies.	L2	PO1, PSO1
CO2	Apply knowledge of automotive sensors and actuators for monitoring and control of vehicle systems.	L3	PO2, PO3, PSO2
CO3	Analyze vehicle motion control systems including cruise control, ABS, traction control, and electronic suspension systems.	L4	PO3, PO4, PO7, PSO2

CO4	Evaluate electronic fuel injection and ignition systems based on performance, efficiency, and control strategies.	**L5**	**PO1, PO2, PO3, PO4, PO5, PO6, PSO2, PSO3**
CO5	Design integrated automotive electronic control systems including digital engine control, onboard diagnostics, and emission control systems.	**L6**	**PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PSO1, PSO2, PSO3**

REFERENCES:

1. *B. Ribbens, "Understanding Automotive Electronics", Butterworth-Heinemann, Eighth Edition, 2017.*
2. *Robert Bosch GmbH (Ed.) Bosch, "Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", Fifth edition, John Wiley & Sons Inc., 2007..*
3. *Tom Denton, "Automobile Electrical and Electronic Systems", Taylor & Francis, Fifth Ediition, 2018.*
4. *Tom Weather Jr and Cland C.Hunter, " Automotive Computers and Control System". Prentice Hall Inc., 1984.*
5. *William B. Ribbens, "Understanding Automotive Electronics", Seventh Edition, Elsevier Publishing, 2012.*

COURSE ARTICULATION MATRIX:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	-	2	3	-	-	-	-	-	-	-	-	-	2	-
CO3	-	-	2	3	-	-	2	-	-	-	-	-	3	-
CO4	2	2	2	3	3	2	-	-	-	-	-	-	3	3
CO5	1	3	3	2	3	2	2	2	2	-	-	-	2	3
25AEOE01	2	2	3	3	3	2	2	2	2	2	2	3	3	3

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEOE02	Subject Title	SENSORS AND ACTUATORS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	III
Prerequisites	Fundamentals of Instrumentation and Measurements		

OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors and actuators with its usage.
- Study State-of-the-art digital and semiconductor sensors.

INTRODUCTION TO MEASUREMENT SYSTEMS (9 HOURS)

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static and dynamic characteristics of measurement systems, zero-order, first-order, and second-order measurementsystems and response.

RESISTIVE AND REACTIVE SENSORS (9 HOURS)

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light- dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning forreactance-based sensors & application to LVDT.

SELF-GENERATING SENSORS (9 HOURS)

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-driftamplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS (9 HOURS)

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to- digital and digital-to-resolver converters.

DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS (9 HOURS)

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, MOSFET transistors, CCD imaging sensors, ultrasonic sensors, Fiber-optic sensors.

TOTAL :45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of measurement systems, sensor classification, and the static and dynamic characteristics of measurement systems.	L2	PO1, PO2, PO4, PSO1

CO2	Apply the operating principles and signal conditioning techniques of resistive and reactive sensors to solve measurement problems.	**L3**	PO1, PO2, PO3, PO4, PO5, PSO1
CO3	Analyze the characteristics, performance, and signal conditioning methods of self-generating sensors for engineering applications.	**L4**	PO1, PO2, PO3, PO4, PO5, PSO1, PSO2
CO4	Evaluate the drive characteristics and performance of actuators for suitable industrial automation and control applications.	**L5**	PO1, PO2, PO3, PO4, PO5, PO6, PSO1, PSO3
CO5	Design and recommend suitable digital and semiconductor-based sensor systems for modern instrumentation applications.	**L6**	PO1, PO2, PO3, PO4, PO5, PO6, PSO1, PSO2, PSO3

REFERENCES:

1. *D. Johnson, "Process Control Instrumentation Technology", 8th Ed, 2014, John Wiley and Sons.*
2. *Clarence W. De Silva, Sensors and Actuators: Engineering System Instrumentation, 2nd Edition, 2015.*
3. *Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.*
4. *Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.*
5. *Princeton Brown, Sensors and Actuators, Published by Library Press, 2017.*

COURSE ARTICULATION MATRIX:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	1	1	1	-	-	-	-	-	3	1	1
CO2	3	2	2	2	-	2	-	-	-	-	-	3	2	1
CO3	3	3	3	1	1	-	-	-	-	-	-	3	2	2
CO4	2	3	3	2	-	1	-	-	-	-	-	3	1	2
CO5	3	3	2	2	2	1	-	-	-	-	-	3	2	2
25AEOE02	3	3	2	1	-	1	-	-	-	-	-	3	2	2

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEOE03	Subject Title	PCB DESIGN
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	III
Prerequisites	Electronic Components and PCB Basics		

OBJECTIVES:

- Understand the need for PCB Design and steps involved in PCB Design and Fabrication process.
- Familiarize Schematic and layout design flow using Electronic Design Automation (EDA) Tools.
- Understand basic concepts of transmission line, crosstalk and thermal issues
- Design (schematic and layout) PCB for analog circuits, digital circuits and mixed circuits.
- Schematic creation & interpretation

INTRODUCTION TO PRINTED CIRCUIT BOARD (9 HOURS)

Introduction to Printed circuit board: fundamental of electronic components, basic electronic circuits, Basics of printed circuit board designing: Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork. Introduction to EOL,ROHS

DESIGN RULES FOR PCB (9 HOURS)

Design rules for PCB: Design rules for Digital circuit PCBs, Analog circuit PCBs, high frequency and fast pulse applications, Power electronic applications, Microwave applications, **PCB Technology Trends:** Multilayer PCBs. Multiwire PCB, Flexible PCBs, Surface mount PCBs, Reflow soldering, Introduction to High-Density Interconnection (HDI) Technology.

INTRODUCTION TO ELECTRONIC DESIGN AUTOMATION(EDA) TOOLS FOR PCB DESIGNING (9 HOURS)

Introduction to Electronic design automation(EDA) tools for PCB designing: Design and simulation of PCB Using EDA tools, Selecting the Components Footprints as per design, Making New Footprints, Assigning Footprint to components, Net listing, PCB Layout Designing, Auto routing and manual routing. Assigning specific text (silkscreen) to design, Creating report of design, creating manufacturing data (GERBER) for design.

INTRODUCTION PRINTED CIRCUIT BOARD PRODUCTION TECHNIQUES (9 HOURS)

Introduction printed circuit board production techniques: Photo printing, film-master production, reprographic camera, basic process for double sided PCBs photo resists, Screen printing process, plating, relative performance and quality control, Etching machines, Solders alloys, fluxes, soldering techniques, Mechanical operations.

PCB DESIGN FOR EMI/EMC (9 HOURS)

PCB design for EMI/EMC: Subsystem/PCB Placement in an enclosure, Filtering circuit placement, decoupling and bypassing, Electronic discharge protection, Electronic waste; Printed circuit boards Recycling techniques, Introduction to Integrated Circuit Packaging and footprints, NEMA and IPC standards.

TOTAL : 45 PERIODS

Upon the completion of this course, students will demonstrate the ability to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals, types, classes, design flow, and fabrication process of Printed Circuit Boards (PCBs).	L2	PO1, PO2, PO3, PO8, PSO1, PSO3

CO2	Apply schematic capture, component selection, footprint assignment, and PCB layout techniques using Electronic Design Automation (EDA) tools.	**L3**	PO1, PO2, PO3, PO5, PO8, PSO1, PSO3
CO3	Analyze PCB design rules, signal integrity, EMI/EMC issues, thermal management, and manufacturing constraints for different applications.	**L4**	PO1, PO2, PO3, PO4, PO5, PO8, PSO1
CO4	Evaluate PCB fabrication techniques, quality control methods, multilayer, SMT, HDI technologies, and PCB production processes.	**L5**	PO1, PO2, PO3, PO5, PO8, PSO1
CO5	Design and develop schematic and PCB layouts for analog, digital, and mixed-signal electronic circuits considering industry standards and manufacturability.	**L6**	PO1, PO2, PO3, PO4, PO5, PO8, PSO1, PSO3

REFERENCES:

1. *Printed Circuits Handbook, Sixth Edition, by Clyde F. Coombs, Jr, Happy T. Holden, Publisher: McGraw-Hill Education Year: 2016*
2. *Complete PCB Design Using OrCAD Capture and PCB Editor, Kraig Mitzner Bob Doe Alexander Akulin Anton Suponin Dirk Müller, 2nd Edition 2009.*
3. *Introduction to System-on-Package, Rao R ,Tummala,& Madhavan Swaminathan, McGraw Hill, 2008*
4. *Printed circuit board design ,fabrication assembly and testing By R. S. Khandpur, Tata McGraw Hill2006*
5. *EMC and Printed circuit board ,Design theory and layout, Mark I Montrose IEEE compatibility society*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	3	3	1	-	-	-	-	3	-	-	-	3	-	1
CO2	3	2	1	-	-	-	-	3	-	-	-	3	-	1
CO3	3	3	1	-	-	-	-	3	-	-	-	3	-	1
CO4	3	2	1	-	-	-	-	3	-	-	-	3	-	1
CO5	3	3	1	-	-	-	-	3	-	-	-	3	-	1
25AEOE03	3	3	1	-	-	-	-	3	-	-	-	3	-	1

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25AEOE04	Subject Title	MICRO ELECTRO MECHANICAL SYSTEMS
Category	Professional Elective	L-T-P-C	3-0-0-3
Regulation	2025	Semester	III
Prerequisites	Basic Microfabrication and Manufacturing Processes		

OBJECTIVES:

- To understand the operation of sensors and actuators.
- To understand the operation of major classes of MEMS devices/systems.
- To give the fundamentals of standard micro fabrication techniques and processes.
- To understand the unique demands, environments and applications of MEMS devices.
- To understand RF MEMS, Bio MEMS and MOEMS.

INTRODUCTION TO MEMS (9 HOURS)

Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Electrical and Mechanicalconcepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection.

SENSORS AND ACTUATORS (9 HOURS)

Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor Piezoresistive sensors – Piezoresistive sensor materials - piezoelectric effects – piezoelectric materials-Stress analysis of mechanical elements – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Thermal Bimorph - Applications – Magnetic Actuators – Micromagnetic components

MICROMACHINING (9 HOURS)

Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies –Basic surface micro machining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – LIGA Process - Assembly of 3D MEMS – Foundry process.

POLYMER AND OPTICAL MEMS (9 HOURS)

Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films, Micro System fabrication– Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS

OVERVIEW OF MEMS AREAS (9 HOURS)

Bonding techniques for MEMS: Surface bonding, Anodic bonding, Silicon - on - Insulator, wire bonding, Sealing – Assembly of micro systems- RF MEMS - switches, active and passive components, Bio MEMS - Microfluidics, Digital Micro fluidics, Ink jet printer, - MOEMS – optical switch, optical cross-connect, tunable VCSEL, micro bolometers

TOTAL : 45 PERIODS

Upon the course completion, the student will have the ability

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the operating principles, characteristics, and applications of MEMS sensors and actuators.	L2	PO3, PO8, PSO3

CO2	Apply scaling laws, material properties, and mechanical principles in the analysis of MEMS devices and microsystems.	**L3**	PO4, PO9
CO3	Analyze microfabrication techniques, micromachining processes, and materials used for the fabrication of MEMS devices.	**L4**	PO2, PO6, PO8, PSO2
CO4	Evaluate polymer MEMS, optical MEMS, fabrication processes, and bonding techniques for selecting suitable MEMS technologies.	**L5**	PO10
CO5	Design MEMS-based solutions by integrating RF MEMS, BioMEMS, and MOEMS concepts for advanced engineering applications.	**L6**	PO11, PSO3

REFERENCES:

1. *Stephen D Senturia, 'Microsystem Design', Springer Publication, 2005.*
2. *Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2012*
3. *Marc J. Madou, 'Fundamentals of Microfabrication: The Science of Miniaturization', 2nd Edition, 2002.*
4. *Nadim Maluf, Kirt Williams, "An Introduction to Microelectromechanical Systems Engineering", 2nd Edition, Artech House, 2004.*
5. *Mohamed Gad-el-Hak, "MEMS Design and Fabrication", CRC press, 2019.*

COURSE ARTICULATION MATRIX

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	-	2	-	-	-	-	2	-	-	-	-	-	3
CO2	-	-	-	2	-	-	-	-	2	-	-	-	-	-
CO3	-	2	-	-	-	3	-	1	-	-	-	-	2	-
CO4	-	-	-	-	-	-	-	-	-	2	-	-	-	-
CO5	-	-	-	-	-	-	-	-	-	-	1	-	-	-
25AEOE04	-	2	2	2	-	3	-	1	2	2	1	-	2	3

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

AUDIT COURSES

Subject Code	25ZAC001	Subject Title	DISASTER MANAGEMENT
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Society, Sustainability, and Environmental Issues		

OBJECTIVES:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and human multiple perspectives tarian response
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

INTRODUCTION (5 HOURS)

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

REPERCUSSIONS OF DISASTERS AND HAZARDS (5 HOURS)

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks of Disease And Epidemics, War And Conflicts.

DISASTER PRONE AREAS IN INDIA (5 HOURS)

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

DISASTER PREPAREDNESS AND MANAGEMENT (5 HOURS)

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

RISK ASSESSMENT (5 HOURS)

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

DISASTER MITIGATION (5 HOURS)

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TOTAL :30 PERIODS

Upon completion of this course, the students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts, types, causes, and impacts of natural and man-made disasters and their significance in disaster management.	L2	PO1, PO4, PO8
CO2	Apply disaster preparedness, mitigation, and management strategies to reduce disaster risks in different scenarios.	L3	PO6, PO9

CO3	Analyze disaster-prone regions, hazards, vulnerabilities, and preparedness plans using risk assessment techniques.	**L4**	**PO2, PO8**
CO4	Evaluate disaster monitoring systems, early warning mechanisms, and disaster response plans for effective emergency management.	**L5**	**PO10**
CO5	Develop disaster risk reduction and mitigation strategies by integrating best practices, community participation, and disaster management policies.	**L6**	**PO10, PO11**

REFERENCES:

1. *R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal book Company.*
2. *Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.*
3. *Goel S. L., Disaster Administration And Management Text And Case Studies", Deep &DeepPublication Pvt. Ltd., New Delhi.*

COURSE ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	3	-	-	2	-	-	-	2	-	-	-	-	-	-
CO2	-	-	-	-	-	3	-	-	2	-	-	-	-	-
CO3	-	2	-	-	-	-	-	1	-	-	-	-	-	-
CO4	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO5	-	-	-	-	-	-	-	-	-	-	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZAC002	Subject Title	ENGLISH FOR RESEARCH PAPER WRITING
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Technical Writing Fundamentals		

OBJECTIVES:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title

PLANNING AND PREPARATION (5 HOURS)

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences,Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

RESEARCH FINDINGS (5 HOURS)

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism,Sections of a Paper, Abstracts. Introduction

LITERATURE REVIEW (5 HOURS)

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

PAPER WRITING SKILLS-I (5 HOURS)

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills areneeded when writing an Introduction, skills needed when writing a Review of the Literature,

PAPER WRITING SKILLS-II (5 HOURS)

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL :30 PERIODS

After completion of this course, the student will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the principles of technical writing and apply appropriate grammar, vocabulary, and academic writing conventions to prepare technical reports and research proposals.	L2	PO4
CO2	Apply literature review techniques, paraphrasing, citation practices, and plagiarism prevention while preparing scholarly documents.	L3	PO5
CO3	Develop a well-structured research paper by organizing its sections, presenting research findings effectively, and following standard publication guidelines.	L6	PO9

REFERENCES:

1. *Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)*
2. *Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press*
3. *Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman''s book .*
4. *Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht HeidelbergLondon, 2011*

COURSE ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	-	-	2	-	-	-	-	-	-	-	-	-	-
CO2	-	-	-	-	2	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	1	-	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZAC003	Subject Title	VALUE EDUCATION
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Social responsibility and human values		

OBJECTIVES:

- To understand value of education and self- development
- To Imbibe good values in students
- To know about the importance of character

ETHICS (6HOURS)

Values and self-development – Social values and individual attitudes. Work ethics, Indian vision ofhumanism. Moral and non- moral valuation. Standards and principles. Value judgements

ELEMENTS OF VALUE EDUCATION (6HOURS)

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature

PERSONALITY DEVELOPMENT (6HOURS)

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity anddiscipline.

DIFFERENT VALUES (6HOURS)

Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Awareof self-destructive habits. Association and Cooperation. Doing best for saving nature

CHARACTER AND COMPETENCE (6HOURS)

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TOTAL :30 PERIODS

After completion of this course, the student will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of human values, ethics, self-development, and their importance in personal and professional life.	**L2**	**PO9**
CO2	Apply ethical principles, social values, and positive attitudes for developing responsible behavior and professional conduct.	**L3**	**PO10**
CO3	Develop personal character, self-discipline, leadership qualities, and value-based approaches for individual and social well-being.	**L6**	**PO1**

REFERENCES:

1. *Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford UniversityPress, New Delhi*

COURSE ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	-	-	-	-	-	-	-	3	-	-	-	-	-
CO2	-	-	-	-	-	-	-	-	-	2	-	-	-	-
CO3	1	-	-	-	-	-	-	-	-	-	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZAC004	Subject Title	PEDAGOGY STUDIES
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Educational Psychology and Learning Theories		

OBJECTIVES:

- To Review existing evidence on the review topic to inform programme design and policy making undertaken by the HRD, other agencies and researchers.
- To Identify critical evidence gaps to guide the development.

INTRODUCTION AND METHODOLOGY (6HOURS)

Aims and rationale – Policy background – Conceptual framework and terminology – Theories of learning, Curriculum, Teacher education – Conceptual framework – Research questions – Overview of methodologyand Searching

THEMATIC OVERVIEW (6HOURS)

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. –Curriculum – Teacher education.

EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES (6HOURS)

Evidence on the effectiveness of pedagogical practices – Methodology for the in depth stage: quality assessmentof included studies – How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? – Theory of change – Strength and nature of the body of evidence for effective pedagogical practices – Pedagogic theory and pedagogical approaches –Teachers' attitudes and beliefs and Pedagogic strategies.

PROFESSIONAL DEVELOPMENT (6HOURS)

Alignment with classroom practices and follow up support – Peer support – Support from the head teacher and the community – Curriculum and assessment – Barriers to learning: limited resources and large class sizes

RESEARCH GAPS AND FUTURE DIRECTIONS (6HOURS)

Research design – Contexts – Pedagogy – Teacher education – Curriculum and assessment – Disseminationand research impact.

TOTAL :30 PERIODS

After completion of this course, the student will be able to understand:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of pedagogical practices, curriculum development, teacher education, and learning theories in different educational contexts.	L2	PO1
CO2	Apply evidence-based approaches and research methodologies to evaluate the effectiveness of pedagogical practices and educational strategies.	L3	PO4
CO3	Analyze educational research findings to identify effective teaching practices, curriculum improvements, and future research directions.	L4	PO10

REFERENCES:

1. *Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.*
2. *Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of CurriculumStudies, 36 (3): 361-379.*
3. *Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education researchproject (MUSTER) country report 1. London: DFID.*
4. *Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.*
5. *Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education.Oxford and Boston: Blackwell.*
6. *Chavan M (2003) "Read India: A mass scale, rapid, learning to read" campaign.*
7. *www.pratham.org/images/resource%20working%20paper%202.pdf*

COURSE ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	-	-	2	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	-	1	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZAC005	Subject Title	STRESS MANAGEMENT BY YOGA
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Basic Understanding of Human Body and Fitness		

OBJECTIVES:

- To achieve overall health of body and mind
- To overcome stress

ASHTANGA (6HOURS)

Definitions of Eight parts of yoga.

YAM (6HOURS)

Do`s and Don't's in life: Ahinsa, satya, astheya, bramhacharya and aparigraha

NIYAM (6HOURS)

Do`s and Don't's in life: Shaucha, santosh, tapa, swadhyay, Ishwar pranidhan

ASAN (6HOURS)

Various yoga poses and their benefits for mind & body

PRANAYAM (6HOURS)

Regularization of breathing techniques and its effects-Types of pranayam

TOTAL :30 PERIODS

After completion of this course, the student will be able to understand:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the concepts of Ashtanga Yoga, Yama, Niyama, Asana, and Pranayama for improving physical and mental health.	L2	PO5
CO2	Apply yoga practices and breathing techniques to enhance concentration, efficiency, stress management, and overall well-being.	L3	PO5

REFERENCES:

1. *Janardan Swami Yogabhyasi Mandal, "Yogic Asanas for Group Tarining-Part-I", Nagpur*
2. *Swami Vivekananda, "Rajayoga or conquering the Internal Nature" Advaita Ashrama (PublicationDepartment), Kolkata*

COURSE ARTICULATION MATRIX

CO/P O	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	-	-	-	1	-	-	-	-	-	-	-	-	-
CO2	-	-	-	-	1	-	-	-	-	-	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation **BOS Approval**

Date:

Subject Code	25ZAC006	Subject Title	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Communication and Interpersonal Skills		

OBJECTIVES:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

HOLISTIC DEVELOPMENT OF PERSONALITY (6HOURS)

Neetisatakam – Holistic development of personality: Wisdom (Verses- 19,20,21,22) – Pride &Heroism (Verses- 29,31,32) – Virtue (Verses- 26,28,63,65)

DO'S AND DONT'S (6HOURS)

Neetisatakam – Dont's (Verses- 52,53,59) – Do's (Verses- 71,73,75,78)

APPROACH TO DAY TO DAY WORK AND DUTIES (6HOURS)

Shrimad Bhagwad Geeta : Chapter 2 (Verses 41, 47,48) – Chapter 3 (Verses 13, 21, 27, 35) – Chapter 6 (Verses 5,13,17,23, 35) – Chapter 18 (Verses 45, 46, 48)

STATEMENTS OF BASIC KNOWLEDGE (6HOURS)

Shrimad Bhagwad Geeta: Chapter2 (Verses 56, 62, 68) – Chapter 12 (Verses 13, 14, 15, 16,17, 18)

PERSONALITY OF ROLE MODEL (6HOURS)

Shrimad Bhagwad Geeta: Chapter2 (Verses 17) – Chapter 3 (Verses 36,37,42) – Chapter 4 (Verses18, 38,39) – Chapter18 (Verses 37,38,63)

TOTAL :30 PERIODS

After completion of this course, the student will be able to understand:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the principles of personality development, wisdom, values, and ethical living based on teachings from Neetisatakam and Shrimad Bhagavad Gita.	L2	PO4
CO2	Apply the principles of self-management, duty, discipline, and positive thinking in personal and professional life.	L3	PO5
CO3	Analyze the role of moral values, leadership qualities, and spiritual knowledge in developing a balanced and responsible personality.	L4	PO9

REFERENCES:

1. *Swami Swarupananda "Srimad Bhagavad Gita" by Advaita Ashram (PublicationDepartment), Kolkata*
2. *P.Gopinath, "Bhartrihari"s Three Satakam (Niti-sringar-vairagya)", Rashtriya SanskritSansthanam, New Delhi.*

COURSE ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	PSO1	PSO2	PSO3
CO1	-	-	-	2	-	-	-	-	-	-	-	-	-	-
CO2	-	-	-	-	2	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	1	-	-	-	-	-

1-Low, 2-Moderate (Medium), 3-High

Course Designed By

Name & Designation

BOS Approval

Date:

Subject Code	25ZAC007	Subject Title	ELECTRONIC WASTE MANAGEMENT
Category	Professional Elective	L-T-P-C	2-0-0-0
Regulation	2025	Semester	I & II
Prerequisites	Pollution and Environmental Health Concepts		

OBJECTIVES

- To learn the basics of Electronics wastes and its management techniques
- To assess the environmental and public health issues of E-waste
- To know the process of material recovery from E-waste

OVERVIEW (10 HOURS)

E-waste Overview, E-waste Management Overview

HEALTH ASSESSMENT (10 HOURS)

Environmental and Public health issues, E-waste health risk assessment

RECOVERY FROM E WASTE (10 HOURS)

Recovery of material from E-waste, Material Recovery Process, electronics and LCA, LCA applications for electronics

TOTAL: 30 PERIODS

Upon completion of this course, the students will be able to:

CO	Course Outcome	Bloom's Level	PO's Mapped
CO1	Explain the fundamentals, sources, and management practices of electronic waste.	L2	PO4
CO2	Analyze the environmental and public health impacts associated with electronic waste and its disposal.	L4	PO5
CO3	Explain and evaluate material recovery processes and life cycle assessment (LCA) methods for electronic waste management.	L5	PO9

REFERENCES:

1. *Electronic Waste Management Rules 2016, Govt. of India, available online at CPCB website.*
2. *MSW Management Rules 2016, Govt. of India, available online at CPCB website.*
3. *Scientific literature uploaded by TAs*